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RESEARCH NOTE

# Design and Implementation of Digital Demodulator For Frequency Modulated CW Radar

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*ABSTRACT*

Radar Signal Processing has been an interesting area of research for realization of programmable digital signal processor using VLSI design techniques. Digital Signal Processing (DSP) algorithms have been an integral design methodology for implementation of high speed application specific real-time systems especially for high resolution radar. In recent times, CORDIC algorithm is turned out to be a huge researched outcome for its easy realizability in on-chip design in the field of vector rotated DSP applications. In this paper, we propose a pipelined CORDIC architecture for digital demodulation in high performance, low power frequency modulated CW Radar. A complex Digital Phase Locked Loop (DPLL) has been used for digital demodulation with pipelined CORDIC module as its core processing element. The FPGA implementation of CORDIC based design has been chosen because of its inherent high throughput of system due to its pipelined architecture where latency is reduced in each of the pipelined stage. Substantial amount of resource utilization has been reduced in proposed design. For better loop performance of first order complex DPLL during demodulation, the convergence of the CORDIC architecture is also optimized. Multiplierless BOXCAR filter has been incorporated at the final stage of the design for better information recovery from narrow samples with little energy signal and easy realization. Hardware synthesized result using Cadence design tools are presented.

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## 1. INTRODUCTION

Phase detection is a vital and sensitive process in radar demodulation [1-5], especially in high speed Doppler radar that requires accurate target detection in real time. In general, radar system uses coherent oscillator for Doppler detection as a reference frequency. Voltage controlled oscillator (VCO) is being used in numerous applications in communications systems where analog demodulation is preferred. However, due to inherent non-linearity, it suffers to maintain linearity over the desired frequency range especially in high frequency demodulation process [6-13]. In present decade, digital or mixed signal design based demodulator is widely used for superior performance. To ensure spectral purity over the desired range of frequency, delay locked loop (DLL) [14, 15] or direct digital frequency synthesizers (DDFS) using various methods are being used [16-20]. Phase detection in communication receiver is very much sensitive to quantization noise. This kind of distortion is basically due to bit resolution. Efforts have been made to design a quantization error free pipelined CORDIC [21-26] architecture based digital demodulator for easy implementation on FPGA platform [27, 28]. We have proposed a first order complex Digital Phase Locked Loop (DPLL) for better switching speed, frequency resolution and phase noise compensation compared to classical radar phase detector.

The iterative formulation of CORDIC algorithm was first developed by Jack E. Volder in 1959 [21] for the multiplication, division and computation of

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trigonometric functions like sine, cosine, magnitude and phase with great precision. The key concept of CORDIC algorithm is simply shift and adds. Although the same functions can be implemented using multipliers, variable shift registers or Multiplier and Accumulator (MAC) units. However, CORDIC can implement these functions efficiently while saving enough silicon area which is considered to be a primary design criteria in application specific on chip implementation where high performance and low cost hardware solutions for DSP are required [22].

This paper designs first order complex DPLL for I/Q channel Radar demodulator using pipelined CORDIC architecture. In digital PLL, an adjustable local sine wave generator and phase detector is required. The CORDIC offers the opportunity to calculate the desired trigonometric computation in a simple and efficient way. Due to the simplicity of the involved operations, the CORDIC realization of complex DPLL is well suited for on chip hardware design and its implementation. The analysis of various error sources is necessary for optimal design of system using the CORDIC processor. In DSP systems, signals are required to be quantized and represented in fixed word-length.

A limited word-length results in the round-off noise and degradation of Signal-to-Quantization Noise Ratio (SQNR) performance [24-26, 29]. In general, larger the dynamic range of the signals, more severe is the round-off noise. To reduce the computation error, a processor designer might simply increase the number of iterations and that would be a huge wastage of processing time and power. Therefore, exact computation of word-length is necessary for designing an architecture for CORDIC. If word-length is larger, the computational speed of CORDIC reduces significantly [24].

On the other hand, if we implement with smaller word-length, the design will suffer from danger of overflow. For designing an optimal application specific CORDIC processor for a high performance signal processing system, the choice of word-length and number of iterations in error analysis are needed to be taken into consideration [27]. In this paper, both the problems of overflow and quantization noise have been addressed adequately for the design optimization process.

The remainder of this paper proceeds as follows. In section 2, the conventional CORDIC algorithm is briefly reviewed. Design of pipelined CORDIC and its optimization including design related issues have been discussed in section 3. In section 4, demodulation process using digital Phase-locked loop for phase detection CORDIC processor has been explained. In section 5, errors and effects of non-idealities have been explained. Hardware synthesis and conclusion may be found in sections 6 and 7, respectively.

**TABLE 1**. Pre-Computed Angles

| *I* | $2^{-i} = \tan \alpha_i$ | $\alpha_i = \arctan(2^{-i})$ | $\alpha_i$ in radian |
|---|---|---|---|
| **0** | 1 | 45° | 0.7854 |
| **1** | 0.5 | 26.565° | 0.4636 |
| **2** | 0.25 | 14.063° | 0.2450 |
| **3** | 0.125 | 7.125° | 0.1244 |
| **4** | 0.0625 | 3.576° | 0.0624 |
| **5** | 0.03125 | 1.7876° | 0.0312 |
| **6** | 0.015625 | 0.8938° | 0.0156 |
| **7** | 0.0078125 | 0.4469° | 0.0078 |
| .. | ….. | …….. | ……. |

## 2. REVIEW OF CORDIC ALGORITHM

The theory of CORDIC computation is to decompose the desired rotation angle into the weighted sum of a set of predefined elementary rotation angles. Each of them can be accomplished with simple shift-add operation for a desired rotational angle $\theta$. It can be represented for $M$ iterations of an input vector $(x,y)^T$ setting initial conditions: $x_0=x$, $y_0=y$, and $z_0=\theta$ as $z_f = \theta - \sum_{i=0}^{M-1} \delta_i \alpha_i$ . If $z_f=0$ holds, then $\theta = \sum_{i=0}^{M-1} \delta_i \alpha_i$, *i.e.* the total accumulated rotation angle is equal to $\theta$. $\delta_i$, $0 \le i \le M-1$, denote a sequence of ±1s that determine the direction of each elementary rotation. When $M$ is the total number of elementary rotation angles, $i$-th angle $\alpha_i$ is given by:

$$\alpha_{m,i} = \frac{1}{\sqrt{m}} \tan^{-1}[\sqrt{m} 2^{-s(m,i)}] = \begin{cases} 2^{-s(0,i)} \\ \tan^{-1} 2^{-s(1,i)} \\ \tanh^{-1} 2^{-s(-1,i)} \end{cases} \quad (1)$$

where, $m$=0, 1 and −1 correspond to the rotation operation in linear, circular, and hyperbolic coordinate system respectively. For a given value of $\theta$, the CORDIC iteration is given by:

$$\begin{bmatrix} x_{i+1} \\ y_{i+1} \end{bmatrix} = \begin{bmatrix} 1 & -\delta_i 2^{-i} \\ \delta_i 2^{-i} & 1 \end{bmatrix} \begin{bmatrix} x_i \\ y_i \end{bmatrix} \quad (2)$$

$$z_{i+1} = z_i - \delta_i \alpha_i \quad (3)$$

where, $\alpha_i = \tan^{-1} 2^{-i}$. To bring a unit vector to desired angle θ, the CORDIC algorithm gives known recursive rotations to the vector. The known rotational values are shown in Table 1 as a Pre-Computed angle.

The iterative equation can be written as follows:

$$x_{i+1} = K_i(x_i - y_i \delta_i 2^{-i}) \qquad y_{i+1} = K_i(y_i + x_i \delta_i 2^{-i}) \quad (4)$$

where, $K_i = \cos\left(\arctan 2^{-i}\right) = \sqrt{(1+2^{-2i})}$ is known as gain factor for each iteration. If $M$ iterations are performed,

then scale factor, K, is defined as the multiplication of every $K_i$ .

$$K = \prod_{i=0}^{M-1} K_i = \prod_{i=0}^{M-1} \sqrt{(1+2^{-2i})} \quad (5)$$

The elementary functions sine and cosine can be computed using the rotation mode of the CORDIC algorithm if the initial vector starts at $(|K|,0)$ with unit length. The final outputs of the CORDIC for the given input values $x_0 = 1, y_0 = 0$ and $z_0 = \theta$ are as follows:

$$x_f = K\cos\theta, y_f = K\sin\theta \text{ and } z_f = 0 \quad (6)$$

Since the scale factor is constant for a given number of rotations, $x_0 = 1/K$ can be set to get purely $\sin\theta$ and $\cos\theta$ values.

## 3. PIPELINED CORDIC AND ITS OPTIMIZATION

The purpose of pipelined implementation is to device a minimum critical path. Therefore, this kind of architecture provides better throughput and lesser latency compared to other designs. It is associated with a number of stages of CORDIC Units where each of the pipelined stages consists of a basic CORDIC engine. The CORDIC engines are cascaded through intermediate latches (Figure 1). The shift operations are hardwired using permanent oblique bus connections to perform multiplications by $2^{-i}$ reducing a large silicon area as required by barrel shifters.

The pre-computed angles, as given in Table 1 of $i$-th iteration angle $\alpha_i$ required at each CORDIC engine can be stored at a ROM memory location, are known. Therefore, the need of multiplexing and sign detection is avoided to reduce critical path. The latency of computation is thus depends primarily on the adder used. Since no sign detection is needed to force $z_f = 0$, the carry save adders are well suited in this architecture. The use of these adders reduces the stage delay significantly upto 2ns. The delay can be adjusted by using proper bit-length in the internal shift register. So ultimately the throughput of the architecture is increased to a many fold as the throughput is given by: "1/delay due to a single adder". It implies that speed up factor becomes more than M and latency of the design is M times of the delay of a single adder. It is obvious that if we increase the number of iterations then the latency of the design also will increase significantly. If an iterative implementation of the CORDIC were used, the processor would take several clock cycles to give output for a given input. However, in the pipelined architecture, it converts iterations into pipeline phases. Therefore, an output is obtained at every clock cycle after pipeline stage propagation. Each pipeline stage takes exactly one clock cycle to pass one output. The simulated output of pipelined stages has been clearly shown in Figure 2.

The internal word-length of the CORDIC is higher than the required word-length at the output to combat the quantization errors of the CORDIC block. The internal word-length of the CORDIC should be as low as possible to achieve higher frequency of operation. So, it is very important to find out first of all the required word-length at the output of the CORDIC block. Taking the signal word-length as 9 bits and the word-length of the decisions as 2 bits, a behavioral simulation of the architecture was made in Verilog HDL assuming very high precision for the signals internal to the architecture. It is observed that convergence of CORDIC is better when the output of the CORDIC block is 16 bits precise. Thus, the output of the CORDIC block is taken to be 16 bits (4 bits for integer part + 12 bits for fractional part). The most recurrent problems for a CORDIC implementation are overflow. Since the first tangent value is $2^0 = 1$, then rotation range will be $\left[-\frac{\pi}{2}, \frac{\pi}{2}\right]$.

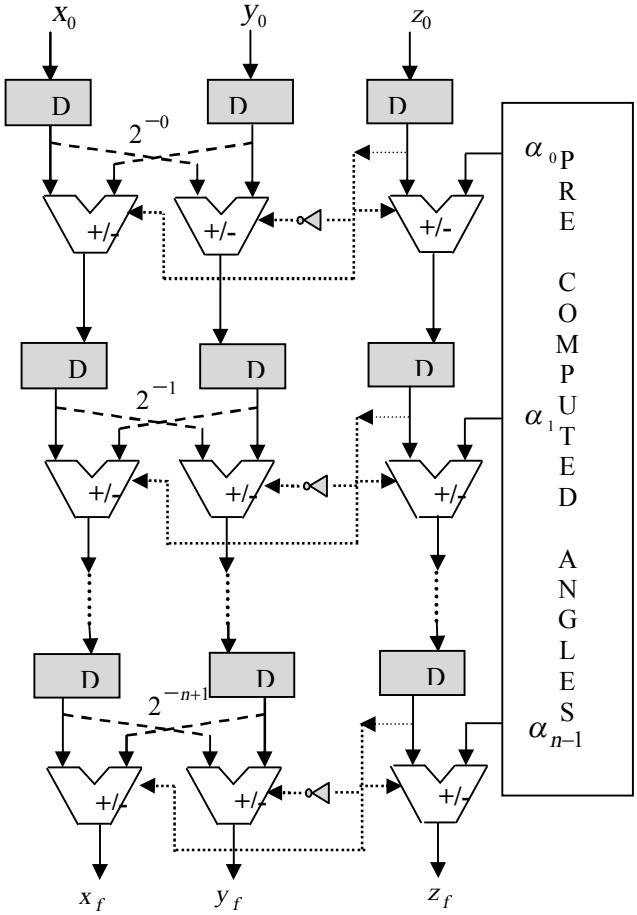


**Figure 1**. Pipelined CORDIC Architecture

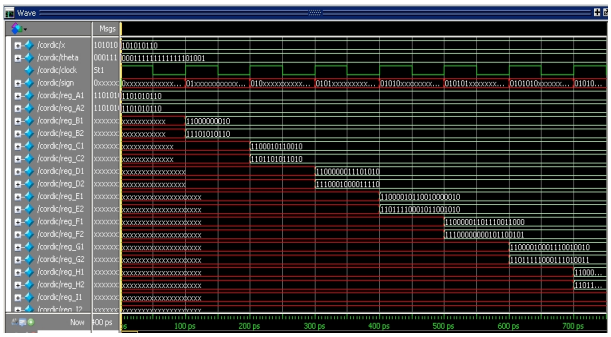

**Figure 2.** Simulation of pipelined stages of CORDIC

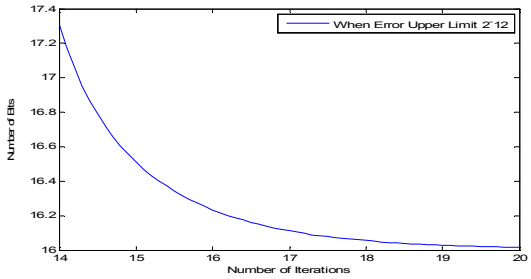


**Figure 3.** Word length in fractional bits Vs number of Iteration

The total error at the output is due to finite word length of the CORDIC block and due to the angle approximation process of the CORDIC algorithm. Firstly, the error due to the angle approximation process will be derived and then the error to the finite word length will be derived. The total error is taken as the summation of the two. The scaling operation also introduces some error which amounts to maximum of $2^{-b}$. So, the final expression for the total quantization error can be given by:

$$\frac{1}{2^{M-1}} * |v^*| + K * \sqrt{2} * 2^{-b}(1 + \sum_{j=0}^{M-1} \prod_{i=j}^{M-1} \sqrt{(1+2^{-2i})}) + 2^{-b} \quad (7)$$

Let the output of the CORDIC block has 12 bits in its fractional part. Therefore, the upper limit of the total quantization error can be taken as $2^{-12}$. Since the required number of fractional bits of the internal word length is 17 when M≥ 17, the optimum value of M would be 17 for the latency to be kept as minimum as possible. The required fractional bits against iterations have been shown in Figure 3. From the figure, it is well understood that 14 numbers of iterations is sufficient for the CORDIC unit to produce almost error free output.

## 4. DIGITAL DEMODULATION TECHNIQUE

The echo from moving target is essentially complex in nature. The complex base band signal is filtered through low pass filter (LPF) inherently holds phase and amplitude information. Our proposed design can easily handle these complex input signals. The phase detector in our design does not produce any image frequency. Therefore, only lower order loop filter is sufficient for the DPLL [28]. This reduces the complexity of already complex DPLL design. The main advantage is that no group delay is caused by the loop filter. Using the vector rotation operator $[x, y]^T \angle\theta$, the complex first-order DPLL demodulator equations for a given input signal can be stated as:

- The real part of the output in phase comparator equation :

$$\varepsilon_n = \Re\{v(n)\angle - \theta_n\} \quad (8)$$

- The loop filter equation is:

$$c_n = 2\pi K_l \varepsilon_n \quad (9)$$

where, $K_l$ is the loop filter coefficient. The loop filter coefficient $K_l$ depends on the sampling frequency and number of iterations of CORDIC algorithm.

- For $M$ number of iterations, the loop filter coefficient $K_l$ can be given by:

$$K_{CORDIC} = \frac{K_l}{\prod_{i=0}^{M-1} \sqrt{1+2^{-2i}}} \quad (10)$$

- The Phase accummulator equation:

$$\theta_{n+1} = (\theta_n + 2\pi K_l \varepsilon_n + \omega_c) \bmod 2\pi \quad (11)$$

where, $\omega_c = 2\pi f_c$ is the center frequency.

The CORDIC based DPLL tries to adjust the continuous phase rotation in such a way that the complex component of the rotated vector will always be zero. Thus, to get the required loop performance, we can set the input signal of the CORDIC as: $\Re\{s(n)\} = x_n$ and $\Im\{s(n)\} = y_n$. The complex digital PLL has been shown in Figure 5. The algorithm, architecture and convergence of the CORDIC have been already discussed. The number of iterations in the CORDIC algorithm determines the speed and accuracy of the CORDIC based Digital PLL. The process of phase detection as discussed earlier needs a reference signal. The in-phase and quadrature channel detection process has been shown through block diagram in Figure 4, whereas input signals are presented in Figure 6. The output can be accumulated at Boxcar generator. Basically, Boxcar technique is a low-pass filtering technique. Implementation of digital filter consists of multiplier and accumulator as a fundamental requirement. Hence, a high speed multiplier is required to work at a sampling speed of Nyquist rate. For

simplicity and easy realizability, multiplier less BOXCAR has been incorporated. Boxcar filter has added advantage over the conventional LPF as far as information recovery from narrow samples with little energy signal is concerned. Low-pass filter averages the signal and produces an output with weak amplitude signals. To avoid this problem, the samples can be stretched for entire inter sample period by increasing their average value before low-pass filter using a sample-and-hold circuit. The circuit is known as Boxcar generator. It raises the sample amplitude at the filter output. Boxcar technique is a low-pass filtering technique. The VLSI implementation of Boxcar generator is very easy as it performs only addition operation. The final phase detected output has been shown in Figure 7 and response of BOXCAR filter has been shown in Figure 8.

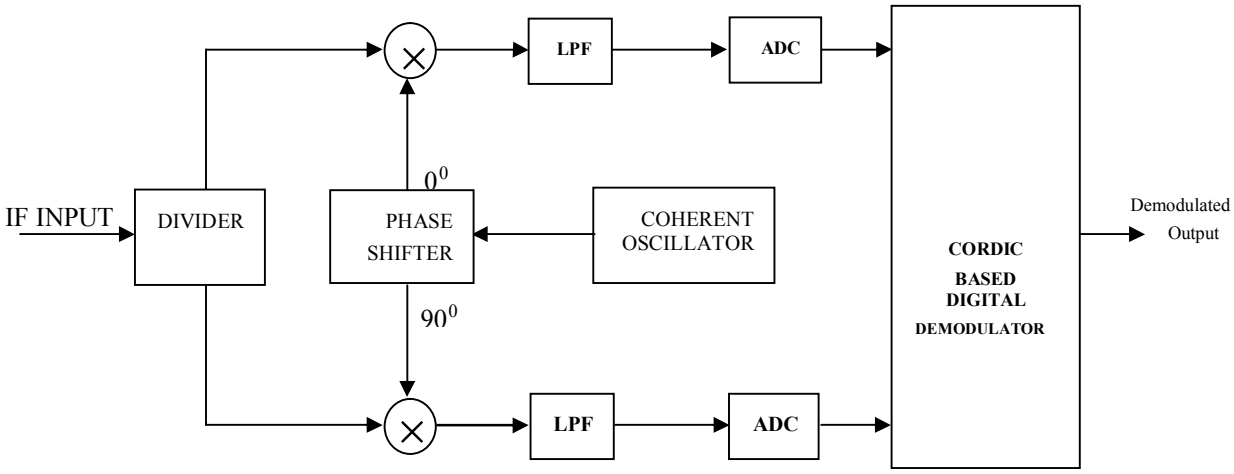


**Figure 4.** CORDIC Based Demodulation in a Simple I/Q Channel Radar Receiver

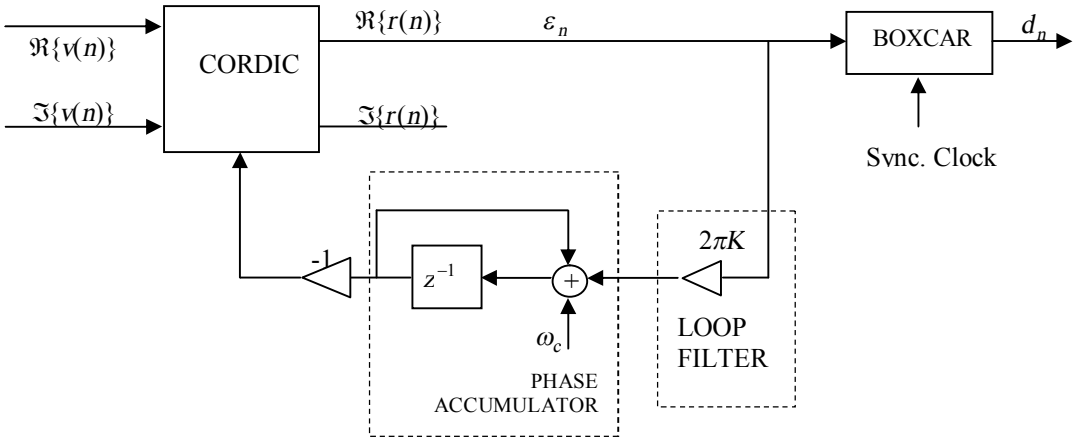


**Figure 5.** Complex digital PLL using CORDIC

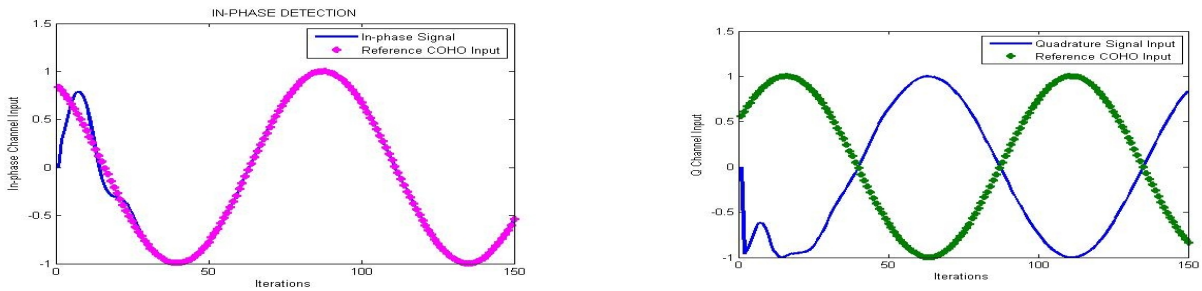


**Figure 6.** I/Q channel phase detection (corresponding input and reference signals)

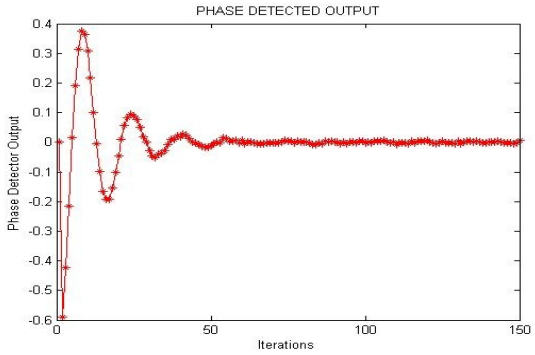


**Figure 7**. Phase Detected Output

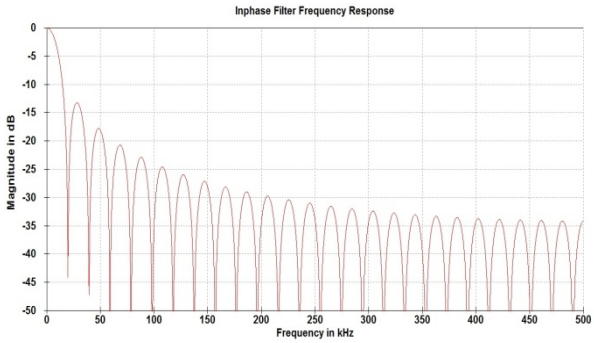


**Figure 8.** The response of BOXCAR filter

## 5. EFFECTS ON DEMODULATION DUE TO NON-IDEALITY OF ADC

The effects of non-ideality of the components used in radar signal processing chain cannot be ignored in efficient phase detection process. For multichannel signal processing, the mismatch in gain and phase always been seen as an expected cause of errors. Apart from this, the quantization and nonlinearity in ADC always affects on its dynamic range [30]. Lets analyze the repercussions of non-ideality in detection process. The dynamic range of ADC, generally equal to channel dynamic range, is equal to:

$$2^{(n_{bit}-1)}q \tag{12}$$

Here, $q$ is quantization step size and $n_{bit}$ is the number of bits (including sign bit). It is a well known fact that in multichannel receiver system, some sort of interferences is occurred due to channel mismatch. The dynamic range of the ADC also gets affected with the expected level of interference power $P_I$.

$$2^{(n_{bit}-1)}q = k\sqrt{P_I} \tag{13}$$

$$q = 2^{-(n_{bit}-1)}k\sqrt{P_I} \tag{14}$$

Here, the guard parameter $k > 1$ is to be selected to avoid saturation. If the input signal is larger than $k\sqrt{P_I}$, the phase detected output will definitely be distorted.

A model for ADC function can help to understand the occurrence of non-ideality. Let $x$ be the scalar Gaussian input of ADC with zero mean and power $\frac{q^2}{12}$. The function of ADC:

$$f_{ADC}(x) = \begin{cases} sf(-x_L) + (1-s)\,f(x) + c, x < -x_L \\ f(x) + c, -x_L \le x \le x_L \\ sf(x_L) + (1-s)\,f(x) + c, x > x_L \end{cases} \tag{15}$$

Where, $f(x) = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3$ is the nonlinear function of ADC. $c$ is offset and $s$ is a parameter that takes its value unity at saturation and otherwise it is zero. The main aim of designer to keep input signal within the interval of $[-x_L, x_L]$ to avoid inevitable saturation. In ideal conditions, the coefficients are kept at $\alpha_1 = 1, \alpha_2 = 0$, $\alpha_3 = 0$, $s = 0$ and $c = 0$ so that $f_{ADC}(x) = x$ become free from any nonlinearities.

In absolute ideal condition ADC follows $f_{ADC}(x) = x$, otherwise it always encountered with some bias. In this condition, it follows with equation $f_{ADC}(x) = mx + b$ which is shown as blue bold line. The bias $b$ and slope $m$ can be computed with the statistical mean squared error (MSE) approximation techniques. Whenever signals falls beyond the linear range i.e. $[-x_L, x_L]$ of ADC response curve as shown in Figure 9, the detection process also gets affected and output of the phase detector also gets corrupted significantly as per non-linearity introduced by ADC. The non-linearity affects on output has been shown in Figure 10.

## 6. HARDWARE SYNTHESIS AND ANALYSIS

The proposed architecture design was synthesized on Spartan-3 based xc3s50pq208-5 FPGA device using XILINX ISE 10.1 and simulated on ModelSim. The area utilization of proposed design is implemented on above said FPGA kit in terms of Sequential, Logic and Inverter. The area consumed by corresponding Sequential, Logic and Inverter circuits are 89 %, 10.8 % and 0.2 %, respectively of available resources as shown in Table 3. The main reason behind less resource utilization is optimization of micro-rotation. The performance of the proposed design has been compared with previously published related works in Table 4. As far as technology, different fabrication process, frequency resolution and so on are concerned, it is very difficult to establish fair comparison between different digital demodulation.

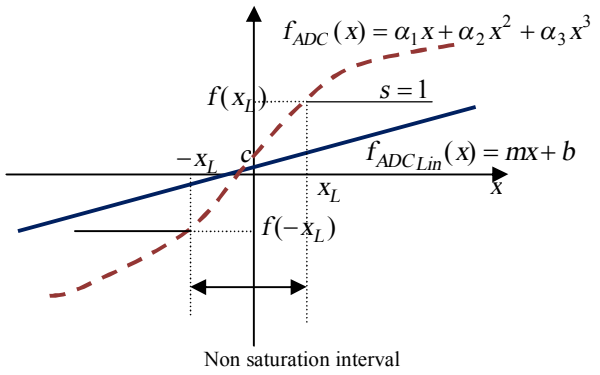


**Figure 9.** Non-linear ADC characteristics with its statistical linearization.

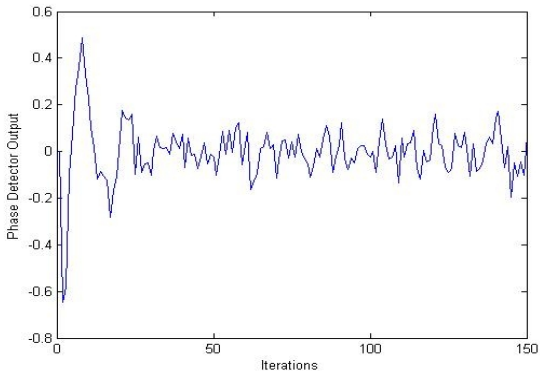


**Figure 10.** Effect on phase detected output due to non-ideality of ADC

**TABLE 2.** Power Measurement

| Leakage Power (nW) | Dynamic Power (nW) | Total Power (nW) |
|---|---|---|
| 263.396 | 115140 | 115403.396 |

**TABLE 3.** Area Utilization

| Type | Instances | Area($\mu m^2$) | Area % |
|---|---|---|---|
| **sequential** | 118 | 7883.568 | 89.0 |
| **inverter** | 2 | 13.306 | 0.2 |
| **logic** | 70 | 958.004 | 10.8 |
| **total** | 190 | 8854.878 | 100.0 |

**TABLE 4**. Performance comparison with other similar published works

| Reference | Process | Power Supply | Power (µW/MHz) | Clock (MHz) | Area ($\mu m^2$) |
|---|---|---|---|---|---|
| Gholami et al. [15] | 180 nm | 1.2 V | 36.5 | 167 | -- |
| Li et al. [17] | 250 nm | 2.5 | 410 | 200 | 720000 |
| Chen et al. [18] | 180 nm | 1.8 V | 160 | 500 | 95000 |
| This Paper | 180 nm | 1.2 V | 115.4 | 211 | 8855 |

## 7. CONCLUDING REMARKS

The paper presents the demodulation technique in a high performance FMCW Radar receiver using an application specific CORDIC processor to facilitate easy and efficient target detection. With using reduced number of micro-rotation and adequate optimized convergence property of CORDIC design, implementation of this kind of demodulator becomes easier. The architecture given in this paper enhances throughput and minimizes latency that facilitates its use in real time signal processing.

Numbers of micro-rotations have been adjusted so as to achieve better loop performance and speed of operation while minimizing quantization error. The property of good convergence of CORDIC is efficiently used in this application.

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# Design and Implementation of Digital Demodulator for Frequency Modulated CW Radar

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**چکیده**

فرایند سیگنال رادار، زمینه تحقیقاتی جالبی برای درک فرایند سیگنال دیجیتال قابل برنامه ریزی شده با استفاده از روش طراحی VLSI می باشد. الگوریتم های فرایند سیگنال دیجیتال (DSP) یک روش طراحی انتگرالی برای اجرای سیستم های ویژه سرعت بالا با زمان واقعی مخصوصا برای رادار با وضوح بالا را دارد. در زمان های اخیر، الگوریتم CORDIC به دلیل آسان بودن درک آن در طراحی روی تراشه (on-chip) در زمینه کاربردهای DSP بردار چرخشی به نتیجه تحقیقاتی بزرگی تبدیل شده است. در این مقاله، ما معماری CORDIC خط لوله ای را برای کشف رمز دیجیتالی در رادار CW با عملکرد بالا و بسامد توان پایین پیشنهاد می کنیم. یک حلقه قفل شده فاز دیجیتالی پیچیده برای کشف رمز دیجیتالی با ماژول CORDIC خط لوله ای به عنوان جزئ فرایندی هسته ای استفاده شده است. اجرای FPGA برای طراحی بر پایه CORDIC به علت توان ذاتی بالای سیستم به دلیل معماری خط لوله ای آن انتخاب شده است، جایی که زمان تاخیر در هر مرحله خط لوله کاهش می یابد. میزان قابل توجهی از استفاده از منابع در طرح پیشنهادی کاهش می یابد. برای عملکرد بهتر DPLLپیچیده درجه اول در مدت کشف رمز، همگرایی معماری CORDIC نیز بهینه شده است. فیلتر BOXCAR در مرحله نهایی طرح برای بازیافت اطلاعات از نمونه های باریک با سیگنال کم انرژی و فهم آسان ترکیب شده است. نتیجه سنتز سخت افزاری با استفاده از ابزارهای طرح Cadence ارائه شده است.

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