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A New Approach for Low Voltage CMOS based on Current-controlled Conveyors

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ABSTRACT

In this paper, a new current-controlled conveyor (CCCII) in complementary metal-oxide semiconductor (CMOS) technology is presented. It features, low supply voltage (±0.7), low power consumption, low circuit complexity, rail to rail operation and wide range parasitic resistance (R_x). The circuit has been successfully employed in a multifunction biquad filter. Simulation results by HSPICE show high performance of the circuit and confirm the validity of the proposed design technique.

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1. INTRODUCTION[1]

Recently, the current-mode (CM) signal processing are receiving much attention [1-18] because it provide solutions for analog circuit problems, showing some advantages with respect to voltage mode (VM) approach [3-5]. In particular, a current mode technique allows realizing analog functions characterized by large bandwidth, non constant gain bandwidth product, and low supply voltage with wide dynamic range. The second generation of current conveyor (CCII), which was introduced in 1970 by Sedra [1], not only is the most important current mode basic building block, but also can operate in both current and voltage-modes, which provides flexibility and enables a variety of circuit designs. The CCII has been used in a wide range of applications varying the range of analog filters, differentiators, integrators, inductance simulator and oscillators. This circuit as a basic building block of function circuit designs adds a tremendous simplification of circuit designs since it can be modeled by simple asymptotic input-output relations. However, the CCII can not control the parasitic resistance at X port (Rx). Therefore, in the most application circuits, it unavoidably requires some external passive resistors which will cause more chip area, consuming high power and without electronic controllability. To solve this problem, the second-generation current-controlled conveyor (CCCII) [7] was introduced which has the advantage of electronic adjustability over the CCII. In CCCII, the parasitic resistance at X port (R_x), can be varied by the current bias which is useful for application such as filters to change its cut off frequency or quality factor. In addition, the use of dual-output current conveyors is found to be useful in some applications using a reduced number of active components [8, 9]. In the last decade, the low voltage circuits became necessary for operation in modern systems like battery supply or portable systems. Rail to rail circuits have a great importance within various circuits that work in low voltage because of utilizing all of voltage headroom. In other hand, in many situations, particularly in mixed analog-digital systems, it is desirable to implement the integrated circuits in complementary metal-oxide semiconductor (CMOS) technology. So, recently, several types of CCII that works at low voltage and rail to rail voltage outputs have been reported in CMOS process [4, 8, 9].

In this work, a new CMOS CCCII with rail-to-rail operation is presented. The proposed circuit can work with low supply potentials while showing low power consumption and high dynamic range. In addition, it can

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provide completely standard functions both in voltage-mode and current-mode. Emphasizing on the use of CCCIIs, a simplified multifunction biquad filter, by employing of two CCCIIs and two capacitors is designed, in which, with appropriately selecting the input signals and without changing circuit topologies completely standard functions can be provided.

The paper organized as follows: Section II describes the basic theory of CCCII. Circuit design of the proposed CCCII structure and application of proposed novel scheme for a biquad filter is presented in section III. Simulation results are described in section IV and conclusion is provided in section V.

2. BASIC PRINCIPLE OF CCCII

The second generation current-controlled conveyor as a current-mode analog building block can be substituted operational amplifiers in varying the range of analog filters, differentiators, integrators, admittance simulator and oscillators. CCCII has three ports, that referred to X, Y and Z. A CCCII like a CCII have two main parts, A voltage follower between X and Y channels and current mirror between X and Z. Hence, the CCCII voltage of port X will trace voltage applied at the port Y. Furthermore, a copy of cureent that is flowing in port X will be appeared at the port Z (equal or in opposite side).

Figure 1 shows the circuit symbol of CCCII, where Y is voltage input with high input impedance, X is voltage trace terminal, Z is current output terminal. I_b denotes bias current that by its adjusting, we can control the voltage relationship between the input terminal and terminal X.

The port relationships of CCCII± can be described by the following matrix representation [3, 15]:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 1 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_x \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

in which, I_x, I_y, I_z are current of ports X, Y and Z, respectively; V_x, V_y, V_y are voltage of aforementioned ports; R_x is the parasitic resistance. Difference between CCCII+ and CCCII– is the direction of the current of Z terminal.

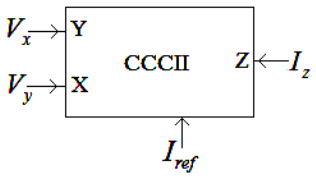


Figure 1. Symbol diagram of a CCCII

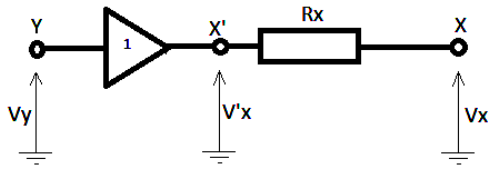


Figure 2. Rule of parasitic resistance (Rx) in CCCII

Now, if the matrix in (1) is expanded, Equation (2) is obtained:

$$I_x = \pm I_z = \pm \frac{V_x - V_y}{R_x} \quad (2)$$

For better explanation, Figure 2 shows the operation of R_x, graphically.

3. CIRCUIT DESIGN

3. 1. Proposed CCCII Figure 3 shows the circuit diagram of the proposed CCCII. In proposed circuitry, there are two parts for negative and positive inputs. Transistors M1-M5 compose positive part, in which transistors M1 and M2 form positive differential pair. Gate of M2 is used for port X and gate of M1 is employed for port Y. The notable point in this scheme is the connection between gate and drain of M2 to prepare low impedance at the node X (diode connection). Transistors M4 and M5 are used for current mirror and active load of above positive differential pair transistors. Similarly, transistors M6-M10, composed negative part, in which transistors M6 and M7 will make negative differential pair and transistors M9 and M10 are employed for active load of negative differential pair transistors. Transistor M3 and M8, as current tail transistors, are used to prepare current biasing for positive and negative differential pairs, respectively. Transistors M15-M17 are current mirror that will make a copy of bias current I_{ref} to M3 and M8. In addition, transistors M11-M14 are employed to prepare a copy of current of port X into port Z.

The drain current of transistor in strong inversion operation will be represented by:

$$I_D = \frac{\beta}{2}(V_{GS} - V_{th})^2 \quad (3)$$

where, I_D is the drain currents and V_{GS} is the gate-to source voltage of transistor, V_{th} stand for threshold voltage; and $\beta = \frac{\mu C_{ox} W}{L}$ is transistors gain factor.

Using Equation (3), difference between input nodes X and Y of CCCII in Figure 4 will be calculated as:

$$V_X - V_Y = V_{GS,x} - V_{GS,y} = \sqrt{\frac{2}{\beta}}\left(\sqrt{I_{Dx}} - \sqrt{I_{Dy}}\right) \quad (4)$$

in which, $V_{GS,x}$, $V_{GS,y}$ are gate-to-source voltages of input differential transistors that their gates are connected via nodes X and Y and I_{DX} and I_{DY} are drain current of foresaid transistors. Using KCL at port X and because of existence the current mirror at the load of differential inputs will give:

$$I_x = I_{Dx} - I_{Dy} \quad (5)$$

Evidently, with positive I_x currents, this current will flow trough positive differential pair transistors (M1-M5) and with negative I_x currents, this current will pass trough negative differential pair transistors (M6-M10). For the transistors that are connected to ports X and Z, as their gate-to-sources are parallel and with equal voltage, their drains current are equal. So, it results:

$$I_z = I_x \quad (6)$$

Lower end node of ports X, Y, Z are connected together and are injected by current reference I_{ref}, so:

$$I_{Dx} + I_{Dy} + I_{Dz} = I_{ref} \quad (7)$$

Using Equation (5) into Equation (7) gives:

$$2I_{Dx} + I_{Dy} = I_{ref} \quad (8)$$

From Equations (4) and (8), currents I_{Dx} and I_{Dy} will be derived as:

$$I_{Dx} = \frac{I_{ref} + I_x}{3} \quad (9a)$$

$$I_{Dy} = \frac{I_{ref} - 2I_x}{3} \quad (9b)$$

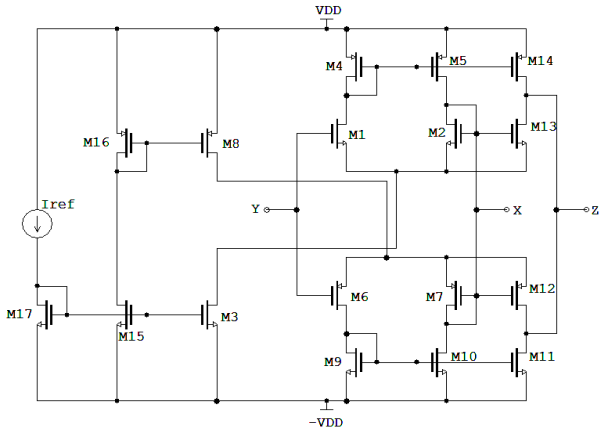


Figure 3. Circuit diagram of the proposed CCCII

Substituting Equation (9) into (4) gives:

$$V_X - V_Y = \sqrt{\frac{2}{\beta}}\left(\sqrt{\frac{I_{ref} + I_x}{3}} - \sqrt{\frac{I_{ref} - 2I_x}{3}}\right) \quad (10)$$

By proper choosing current reference I_{ref}, and for amounts that are much more than current of port X (I_x), the right hand side terms of Equation (10) can be approximated by Taylor series:

$$\sqrt{\alpha \pm \delta} \cong \sqrt{\alpha} \pm \frac{1}{2}\frac{1}{\sqrt{\alpha}}\delta. \quad (11)$$

So, employing Equation (11) into (10) will gives:

$$V_X - V_Y \cong \sqrt{\frac{3}{2\beta I_{ref}}}.I_x \quad (12)$$

and by substituting Equation (12) into (3), parasitic resistance is obtained by:

$$R_X \cong \sqrt{\frac{3}{2\beta I_{ref}}} \quad (13)$$

From Equation (13), the parasitic resistance is adjustable by bias current, which control V_{XY} by bias current.

Hence, Equations (3) and (5) represent second and third rows of Equation (1), respectively. Furthermore, as the node Y is at the high impedance gate of transistors M1 and M6, the current at the port Y is equal to zero ($I_Z = I_X$) which represent first row of Equation (1). In circuit of Figure 3, minimum required supply voltage is $V_{gs} + 2V_{ds}$ which is suitable for low voltage applications. The input voltages at the nodes X and Y can reach up to near supply voltages, so it can be truly assumed that it can work with rail-to-rail operation. In addition, the main circuit of CCCII contains 14 transistors; so, it has low circuit complexity. At last let earn parasitic resistance in small signal (r_x) will be:

$$r_x = \frac{1}{g_{m2}} \| \frac{1}{g_{m7}} \quad (14)$$

in which,

$$g_{m2} = \sqrt{\frac{2}{3}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 I_{ref}} \quad (15a)$$

$$g_{m7} = \sqrt{\frac{2}{3}\mu_p C_{ox}\left(\frac{W}{L}\right)_7 I_{ref}} \quad (15b)$$

So, parasitic resistance in small signal will be obtained by bias current as following:

$$r_x = \frac{1}{\left(\sqrt{\frac{2}{3}\mu_n C_{ox}\left(\frac{W}{L}\right)_2} + \sqrt{\frac{2}{3}\mu_n C_{ox}\left(\frac{W}{L}\right)_2}\right)} \cdot \frac{1}{\sqrt{I_{ref}}} \quad (16)$$

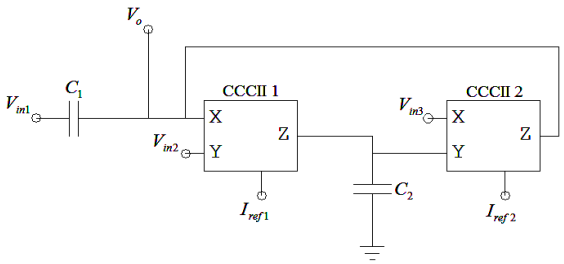


Figure 4. Topology of multifunction filter [4]

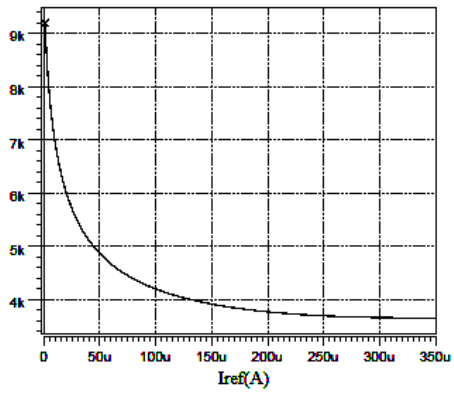


Figure 5. Parasitic resistance R_X vs. current reference I_{ref}

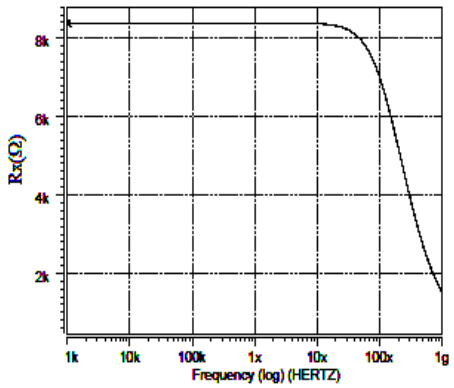


Figure 6. Frequency response of parasitic resistance R_X

TABLE 1. Values of the inputs for different filter

Filter Responses	Input Selection		
Vo	V_{in1}	V_{in2}	V_{in3}
LP	0	1	1
HP	1	0	0
BP (R_{x1}=R_{x2})	0	1	0
AP (R_{x1}=R_{x2})	1	1	2
BR (R_{x1}=R_{x2})	1	1	1

3. 2. Application Example As an application example, an analog biquad multifunction filter depicted in Figure 4 [4] is used to show the characterization of the new CCCII. This topology is very simple and it is composed by just two capacitors and two CCCII. All of function can be obtained with given value to V_{in1}, V_{in2} and V_{in3}. The Transfer function of this multifunction can be represented by:

$$V_o = \frac{s^2 C_1 C_2 R_{x1} R_{x2} V_{in1} + (sC_2 R_{x2} + 1)V_{in2} - sC_2 R_{x1} V_{in3}}{s^2 C_1 C_2 R_{x1} R_{x2} + sC_2 R_{x2} + 1} \quad (17)$$

in which input currents V_{in1}, V_{in2} and V_{in3} can be selected from Table 1 to reach each function of this multifunction. The quality factor Q_o and natural frequency ω_o in all functions of this structure can be expressed as [4]:

$$Q_o = \sqrt{\frac{c_2 R_{x1}}{c_1 R_{x2}}} \quad (18)$$

$$\omega_o = \sqrt{\frac{1}{c_1 c_2 R_{x1} R_{x2}}} \quad (19)$$

So, the cutoff frequency and quality factor of the filter can be adjusted by parasitic resistance (or corresponding to current reference (I_{ref}) of CCCIIs.

4. SIMULATION RESULTS

The specification of CCCII and the multifunction filter are presented here by HSPICE simulation using 0.18µm TSMC CMOS technology. Supply voltages are ±0.7V and capacitors are 100pF. Aspect ratio of transistors is given in Table 2. Figure 5 shows the parasitic resistance R_X of the proposed CCCII versus current bias I_{ref}. It can be seen that the parasitic resistance can be varied from 3.6 to 9.2 kΩ which is wide range variation. Frequency response of parasitic resistance is shown in Figure 6 for current reference of $200\ \mu A$. In order to extract current characteristic of the proposed CCCII Figure 7 is employed. Figure 8 shows current relation of CCCII that its variation is the same as represented in Equation (6). In similar case, Figure 9 is used to extract voltage characteristic of the CCCII. Figure 10 shows variation of V_x versus V_y and for different current biases.

Characteristics of the proposed circuit have been compared with other current controlled conveyors which were presented in [3, 15] and are listed in Table 3. One attempt is to CCCII circuit design based on the BJT transistors [15]. However, in many situations, particularly in mixed A/D systems, it is desirable to implement the circuits in MOS technology. In [3] design of CCCII has been performed in CMOS technology. However, it uses large number of transistors. The minimum supply voltage of this circuit is 3 V_{gs+} V_{ds} and its load suffers from body effect.

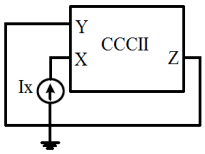


Figure 7. Employed circuit to extract current characteristic

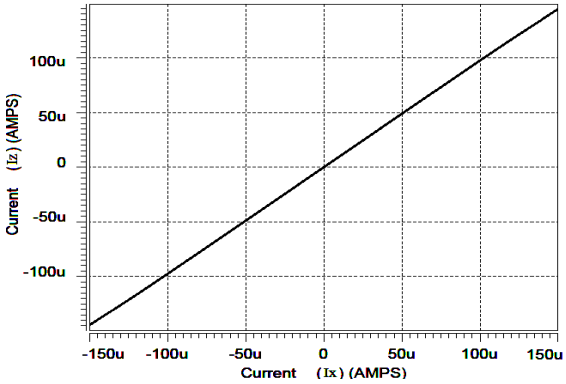


Figure 8. Current characteristic of the proposed CCCII

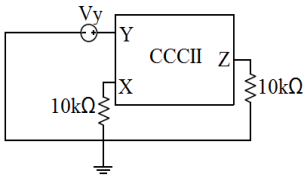


Figure 9. Employed circuit to extract voltage characteristic

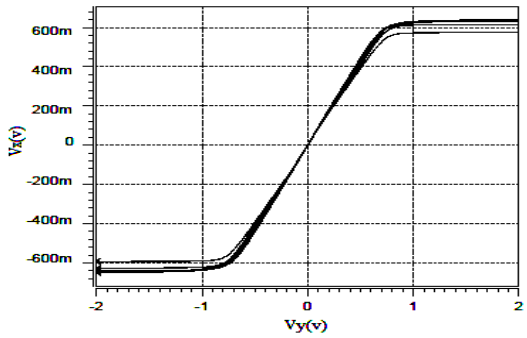
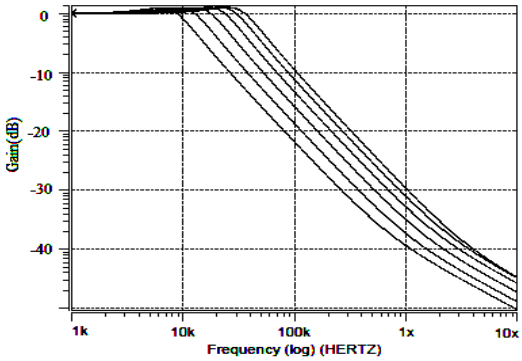


Figure 10. Voltage characteristic of the proposed CCCII



Figuer 11. Natural frequency tuning of low pass filter of multifunction

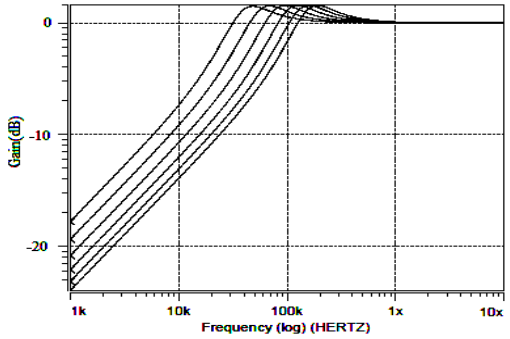


Figure 12. Natural frequency tuning of high pass filter of multifunction

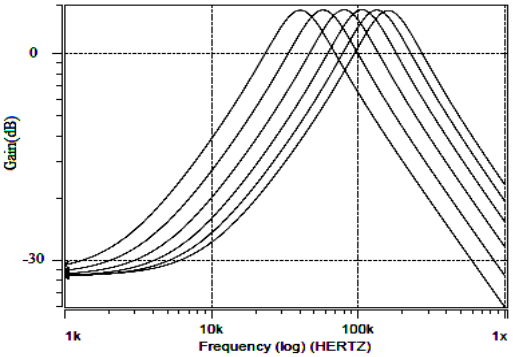


Figure 13. Natural frequency tuning of band pass filter of multifunction

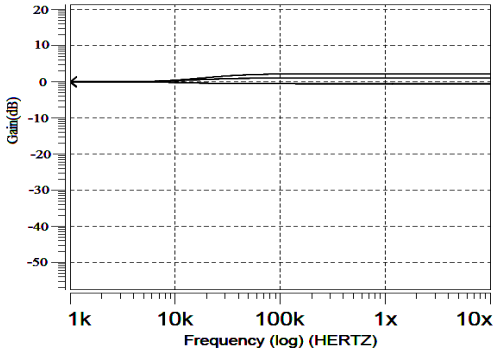


Figure 14. Natural frequency tuning of all pass filter of multifunction

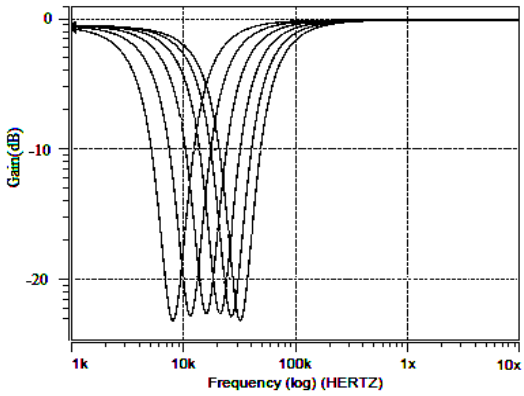


Figure 15. Natural frequency tuning of band reject filter of multifunction

TABLE 2. Aspect ratio of transistors for CCCII

Transistors	$W(\mu m)/L(\mu m)$
M1, M2, M10	17.5/0.18
M3, M4, M11	4.5/0.18
M5, M6, M12, M16, M17	15/0.18
M7, M8, M9, M15	5/0.18
M13	10/0.18
M14	27.5/0.18

TABLE 3. Comparisons parameters

Specification	[3]	[15]	This Work
Transistor type	MOS	BJT	MOS
Voltage follower	Simple Diff. Pair	Trans-Linear	Complementary Diff. Pairs
L (μm)	0.35	N.C.	0.18
Supply voltage (V)	±1.65	±3	±0.7
Circuit complexity (no. of transistors)	54	35	17
Max. Power consumption (mW)	22	6	1.5
R_X (kΩ)	0.7-1.5	N.C.	3.6k -9.2k
Voltage transfer range (V)	-0.9Vdd to +0.9Vdd	N.C.	-Vdd to +Vdd

* Not Commented

In our work, two complementary differential pair has been employed and sources of MOSs are connected together. The minimum supply voltage is $2V_{gs}+2V_{ds}$. Therefore, the body effect is eliminated and also it provides wider input dynamic range, low supply voltage, rail to rail operation, and wide range parasitic resistance (R_x). The circuit complexity (amount of transistors) of this circuit is much lower than those reported in [3, 15]. Furthermore, supply voltage level reduction, lower number of branches with stacked transistors and amount of transistors lead to lower power consumption.

The proposed CCCII, is employed in a multifunction filter that is shown in Figure 4. Figure 11 shows the frequency tuning plot in constant Q, where the value of current biases has been changed equally from $80\mu A$ to $150\mu A$ (plots left to right). It shows that the natural frequency of the filter is varied by changing the current biases. In similar case, Figures 12 to 15 present frequency response for other functions of the multifunction filter. In a similar way, the quality factor tuning achieved in constant ω_0, by multiplication of current reference I_{ref1} with coefficient α, and division of current reference I_{ref2} by coefficient α. Figure 16 shows the quality factor tuning of low pass filter of multifunction using capacitors of 1nF and different value of coefficient α, ranging from 0.1 to 1.8 in linear variation (plots down to up). To examine the nonlinear behavior of the filter, a sinusoidal input voltage with a 2 kHz frequency and varying amplitude is considered for low pass filter. Figure 17 shows Total Harmonic Distortion (THD) of filter. The worst-case THD of the output voltage with a 4096 point Fast Fourier Transform (FFT) was less than -75dB for input voltages that are less than 650mV.

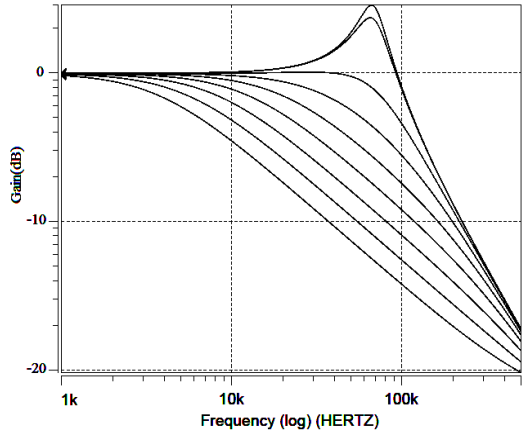


Figure 16. quality factor tuning of low pass filter of multifunction

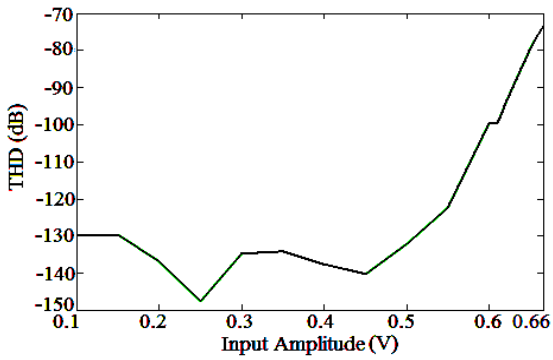


Figure 17. Output total harmonic distortion of the low pass filter

5. CONCLUSION

A CMOS based current-controlled conveyor was introduced for low voltage applications. Simulation results of a biquad multifunction filter employed using the proposed CCCII shows high performance of the proposed circuit. It also confirms the validity of the proposed technique and demonstrate the functionality of the circuit. As a result, an efficient new circuit for CCCII is obtained.

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A New Approach for Low Voltage CMOS based on Current-controlled Conveyors

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چکیده

در این مقاله یک نقال کنترل شونده جریان در تکنولوژی CMOS ارائه شده است. این طرح دارای خواص ولتاژ پایین، توان مصرفی پایین، پیچیدگی کم مداری، عملکرد ولتاژی تا سقف منابع ولتاژی و مقاومت پارازیتی با رنج وسیع می باشد. مدار بصورت موفقیت آموزی در فیلترهای متعامد بکار گرفته شد. نتایج شبیه سازی به کمک نرم افزار HSPICE بازدهی بالای مدار را نشان می دهد و درستی تکنیک طرح پیشنهادی را اثبات می کند.

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