CONTROLLING COMMON-MODE VOLTAGES IN MULTILEVEL INVERTERS

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Abstract This paper proposes a novel method based on pulse width modulation techniques to reduce and control the common-mode voltage in three-phase multilevel inverters. Besides controlling the common-mode voltage, this method is capable of controlling capacitors voltages and load currents with low switching losses and harmonic contents. In fact, due to the existence of different pulse patterns and the possibility of choosing the optimum patterns based on the most important criteria, the controllability of this method has risen properly. Furthermore, the controller randomly selects one of the optimum pulse patterns, which has another advantage of spreading the spectrum contents of the output voltage for low electromagnetic interferences and mechanical vibration. This method can be applied to a three-phase, three-level inverter with the flying capacitor topology. Another advantage of this method is that the technique can be applied to more voltage levels without significantly changing the control algorithm. The simulation results of a five-level inverter in this paper indicate that the proposed technique can be used to implement a multilevel inverter.

Keywords Pulse Width Modulation Techniques, Common-Mode Voltage, Capacitors Voltages, Load Currents, Three-Phase Multi-Level Inverter

چکیده در این مقاله، روشی جدید بر مبنای تکنیک های مدولاسیون پهنای پالس برای کاهش و کنترل ولتاژ حالت مشترک در اینورترهای چند سطحی سه فاز ارائه گشته است. این روش، علاوه بر کنترل ولتاژ حالت مشترک، توانایی کنترل ولتاژ خازن ها و جریان های بار را در کنار محتوای هارمونیکی کم و تلفات سوئیچینگ پایین دارا می‌باشد. به عبارت دیگر، وجود ترکیبات مختلفی از پالس ها، امکان انتخاب حالات بهینه را افزایش داده و موجب کنترل پذیری بهتر ولتاژ حالت مشترک در این روش می‌شود. علاوه بر این، انتخاب طرح پالس نهایی از میان چند طرح بهینه به صورت تصادفی توسط کنترل کننده صورت می‌پذیرد. این امر، موجب پخش شدگی طیف هارمونیکی ولتاژ خروجی می گردد و بدین طریق تداخل های الکترومغناطیسی و لرزش های مکانیکی کاهش می‌یابد. روش مذکور قابل اعمال به اینورتر سه سطحی سه فاز از نوع Flying Capacitor است. یکی دیگر از مزایای این روش آن است که تکنیک فوق را می توان بدون نیاز به تغییرات عمده در الگوریتم کنترل، به سطوح ولتاژی بالاتر نیز اعمال نمود. نتایج شبیه سازی یک اینورتر پنج سطحی در این مقاله، مبین قابل استفاده بودن تکنیک فوق جهت پیاده سازی یک اینورتر چند سطحی می‌باشد.

1. INTRODUCTION

Conventional two-level pulse width modulated (PWM) inverters have the problem of generating high frequency common-mode voltages (CMV) with high dv/dt. This problem creates motor shaft

voltage through electrostatic couplings between the rotor and the stator windings. It also causes motor shaft voltage between the rotor and the frame. Consequently, the shaft voltage results in excessive bearing currents when it exceeds the dielectric capability of the bearing grease. At the same time, the CMV will cause a much larger common-mode leakage current to flow into the ground via electrostatic coupling between the stator windings and the grounded frame. Since this current will eventually flow back to the input terminals through the ground conductor and the power mains, it will cause significant common-mode electromagnetic interference (EMI) emission [2].

The common-mode problems are increased with the use of fast-switching IGBTs in PWM motor drives [3]. The olutions can be broadly divided into those minimizing common-mode currents and those seeking CMV cancellation. Currently, there are many CMV reduction and elimination techniques in literature [2-14]. These studies have been focused on utilization of additional hardware or filter which results in sluggish response and/or bulky circuitry [5-7] or open end motor winding with higher rating of switching devices [2,10]. References [2,10] present a dual- bridge inverter (DBI) to generate zero CMV. Although the motor shaft voltage and the resulting bearing currents are eliminated successfully, a double-winding induction motor becomes necessary [12]. In [5,6], an active filter is proposed to cancel the CMV and reduce ground current and conducted EMI. However, a common mode transformer of significant size has to be used. A space-vector algorithm was proposed in [9] to minimize the neutral-to-ground voltage of the motor stator winding by synchronizing the switching sequence of the rectifier and inverter, which limits the current control capabilities. In [8], a four leg inverter with second order filter approach is presented to reduce the neutral voltage of the filter and effectively reduce the CMV. The results demonstrated a reduction in the filter neutral voltage, although resonance problems did arise in the experimental work due to the numerous energy storage elements presented. In addition, the modulation index is limited to 0.66 [10]. On the other hand, none of these methods consider the switching losses and/or the low frequency harmonics. They may even increase the switching loss [2,12]. Multilevel voltage source inverters are a new generation of inverters. These are suitable for high power and high voltage applications due to reduced harmonic contents and low voltage stress across the load [1,2]. Multilevel inverters have different voltage levels and switching states. They may reduce and control the CMV which assists the generation of a high quality (low harmonic) voltage and current.

The CMV in this paper is defined as the voltage between the common-point in a three phase Y connected R-L load of the inverter and the electrical ground (Figure 1). Mathematically, this can be derived by considering the voltage at each phase of the inverter output with respect to the ground to be equal to the phase-to-a floating point voltage plus the floating point-ground voltage.

$$V_{aX} = V_{an} + V_{nX}$$
$$V_{bX} = V_{bn} + V_{nX}$$
$$V_{cX} = V_{cn} + V_{nX}$$

if the sum average of the three phase output voltage with respect to this assumed floating point under balanced operating condition is zero, then this floating point can be considered as the neutral point of the inventers' output. The voltage across the floating point neutral and ground can then be defined as the common-mode voltage, V_{n-x}.

$$V_{aX} + V_{bX} + V_{cX} = V_{an} + V_{bn} + V_{cn} + 3V_{nX}$$

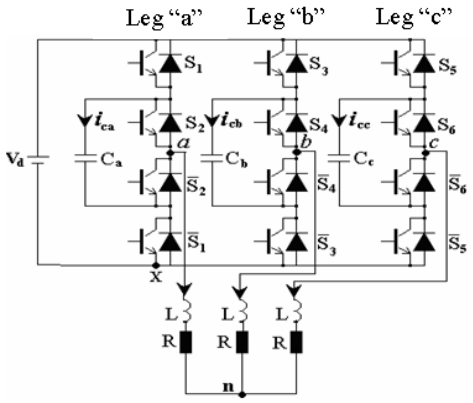


Figure 1. A three-phase three-level inverter with the flying capacitor topology.

$$\Sigma V_{a,b,c-n} = 0$$

$$V_{nX} = \frac{V_{aX} + V_{bX} + V_{cX}}{3}$$

Since the amplitude of the CMV is the average of the branch voltages amplitudes, changing the PWM scheme applying to the switches, can change the branch voltages and consequently control the CMV. In this paper, a new CMV reduction and control technique is proposed for the multilevel inverters which controls the capacitors voltages and load currents with low switching losses and low current ripple.

2. COMMON MODE VOLTAGE REDUCTION AND CONTROL TECHNIQUE

This paper presents a new pulse pattern for a three-phase multilevel inverter with the flying capacitor topology, minimizing and controlling the common mode voltage. This method can be applied to different voltage levels without significantly changing the control algorithm. Multilevel inverters generate different voltage levels. They use capacitors as voltage sources which are placed across the power switches in each leg as shown in Figure 1. This figure shows a three-phase three-level inverter with the flying capacitor topology feeding an inductive-resistive load. The flying capacitors are charged or discharged when the load currents pass through them during operation. In order to operate properly, the controller has to achieve correct switching states to balance the capacitors voltages.

With the capacitors voltages controlled at $\frac{V_d}{2}$, the output voltage of each leg would be a combination of voltages 0, $\frac{V_d}{2}$ and V_d as shown in Figure 2 for leg "a". Table 1 represents different switching states for leg "a". In this table the 0s and 1s indicate the switch is off and on, respectively. As can be seen from the table, there are two switching states (state 01 and state 10) in each leg which result in output voltage $\frac{V_{dc}}{2}$. In these switching states, depending on the load current direction, the capacitors might be charged or discharged. In state $S_1S_2 = 01$ for example, if the load current is positive (negative), capacitor C_a will be discharged (charged). Figure 3 shows the circuit diagram of switching states $S_1S_2 = 01$ and $S_1S_2 = 10$. In this figure, the capacitor C_a will be charged in state $S_1S_2 = 10$, and discharged in state $S_1S_2 = 01$ with positive load current; and reversely with negative load current. These conclusions can be summarized in Table 2.

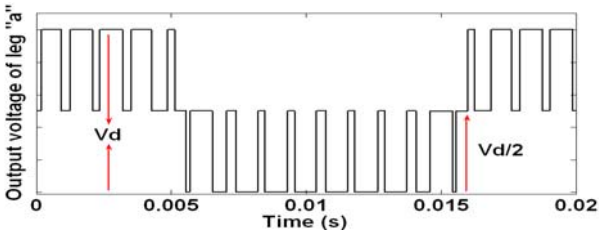


Figure 2. Output voltage of leg "a".

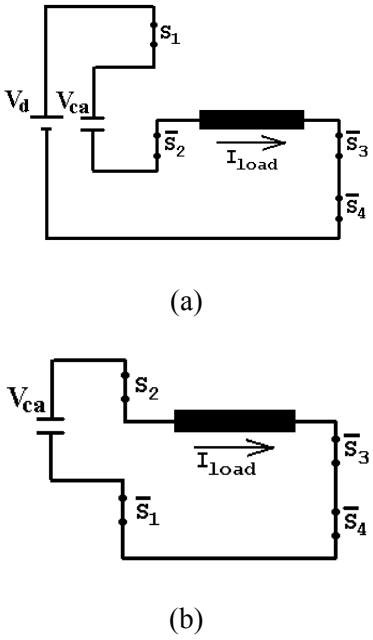


Figure 3. Circuit diagram when the capacitor in leg "a" is (a) charged (state $S_1S_2 = 10$), (b) discharged (state $S_1S_2 = 01$).

TABLE 1. Switching States for Leg "a" in Figure 1.

S_1	S_2	V_{aX}
0	0	0
0	1	$\frac{V_d}{2}$
1	0	$\frac{V_d}{2}$
1	1	V_d

TABLE 2. Switching States for Leg "a" with the C_a Charge and Discharge Considerations.

S_1	S_2	V_{aX}	$I_{load} > 0$ fo V_{ca}	$I_{load} < 0$ for V_{ca}
0	0	0	No Change	No Change
0	1	$\frac{V_d}{2}$	Decrease	Increase
1	0	$\frac{V_d}{2}$	Increase	Decrease
1	1	V_d	No Change	No Change

Generally, when the switching state is selected to generate $\frac{V_d}{2}$, controlling the capacitor voltage at $\frac{V_d}{2}$ should be considered. Consequently, the controller has to measure the capacitor voltage and compare it to the reference value. Depending on the error voltage and the load current sign, one of the switching states (01 or 10) must be chosen using the adjacent voltage vectors law which minimizes the switching losses.

In general, a modulation scheme, such as the space vector modulation (SVM), generates the output voltage based on duty cycles corresponding to the average voltage of the sampled reference voltage or current. In multilevel inverters, there are more than two voltage levels in each switching cycle, so that different PWM schemes can generate the appropriate output voltages. So the output voltage and the CMV can be controllable due to these different schemes. In existing CMV reduction methods in multilevel inverters, in the process of generating the output voltage, the CMV is cancelled, but these methods do not consider the switching losses or low order harmonic contents [12]. In the proposed method, the switching states are selected based on the following algorithm to minimize CMV in a three-level three-phase inverter:

- If duty cycle of each leg is in the range of [0.5,1], the output voltage level is considered between $\frac{V_{dc}}{2}$ and V_{dc}.
- If duty cycle of each leg is in the range of [0,0.5], the output voltage level is considered between 0 and $\frac{V_{dc}}{2}$.

In the proposed method, three pulse positions are defined as shown in Figure 4, where the pulse can be placed at the beginning, center or end of each switching cycle of a phase.

Consequently there are 27 different pulse combinations in each switching cycle of all three phases. Since the CMV is defined as the average voltage of leg voltages ($V_{cm} = \frac{V_{aX} + V_{bX} + V_{cX}}{3}$), the CMV will also have 27 different voltage shapes in each switching cycle. This average voltage results in a 7-level CMVs: $(\frac{6}{3}\times\frac{V_d}{2})$, $(\frac{5}{3}\times\frac{V_d}{2})$, $(\frac{4}{3}\times\frac{V_d}{2})$, $(\frac{3}{3}\times\frac{V_d}{2})$, $(\frac{2}{3}\times\frac{V_d}{2})$, $(\frac{1}{3}\times\frac{V_d}{2})$ and 0. Since in measuring the common-mode voltages, the midpoint of the dc bus is considered as the reference point, these 7 levels can be rewritten as: $(\frac{3}{3}\times\frac{V_d}{2})$, $(\frac{2}{3}\times\frac{V_d}{2})$, $(\frac{1}{3}\times\frac{V_d}{2})$, (0), $(\frac{-1}{3}\times\frac{V_d}{2})$, $(\frac{-2}{3}\times\frac{V_d}{2})$, $(\frac{-3}{3}\times\frac{V_d}{2})$. It needs to be noted that more than one combination of the 27 different pulse combinations may have a lower value of CMV in comparison with other switching states. These patterns do not

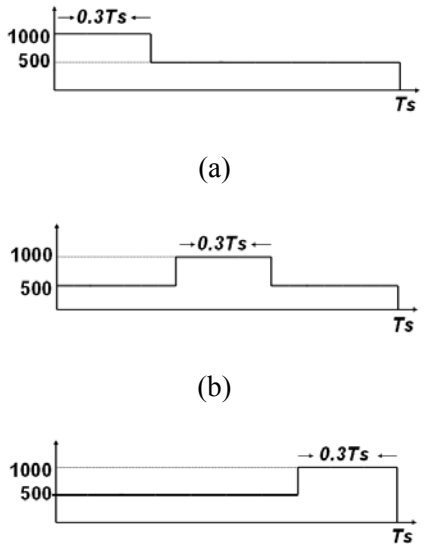


Figure 4. Three different shapes of a pulse with duty cycle = 0.65.

have any difference in reducing the CMV value and do not fully cancel the common mode voltage, but they can reduce and control the common mode voltage to a minimum level. In other words, if we want to fully cancel the CMV, some other issues such as low switching losses and current ripple can not be controlled properly. The novelty of this work is to present a method to reduce and control the CMV while the other important issues are optimized.

In the proposed method, three different pulse patterns are used for each leg and the controller achieves the optimum pulse pattern within 27 combinations based on the following criteria:

- Low switching losses (using adjacent voltage vector),
- Capacitor voltage control (using a correct switching state and based on load current),
- Low CMV (shifting the pulse position in such a way to generate low CMV and less zero vectors (00,00,00), (11,11,11)),
- Low leakage current and load current ripple (a random selection of the best centering pulse position within the achieved pulses).

Thus, based on the pulse width modulation technique, the controller calculates the duty cycle to generate the output voltage; the pulse patterns are selected in such a way to minimize the common mode voltage according to Figure 5; the controller achieves the proper switching states in order to control the capacitor voltage based on the adjacent voltage vector and the load current sign; the final pulse pattern is selected based on the best centering pulse position which improves the load current ripple and also minimize dv/dt corresponding to low leakage current. Figure 6 shows steps for this procedure in a flowchart. In fact centering the pulse pattern is the main criteria for improving the load current ripple. The controller analyses all of the above-mentioned pulse combinations to find the optimal case by considering the load current harmonic factor as an important issue. There could be more than one combination among the chosen cases that have a better harmonic spectrum compared to other combinations. These are the cases that have more pulses at the center in their switching cycles, for example see case (b) in Figure 4). Finally, the desired case will be randomly chosen from the above cases to apply to the system.

For example, Figure 5 shows three different pulse positions where the case (a) shows the traditional pulse centering which has the lowest current ripple but a higher common mode voltage; while the case (b) has the lower common mode voltage but the pulse pattern is not in such a case to generate a low current ripple. The case (c) shows an optimum case, where the pulse in leg "a" is placed at the beginning of the switching cycle and the pulses in legs "b" and "c" are placed at the center which gives the lower common mode

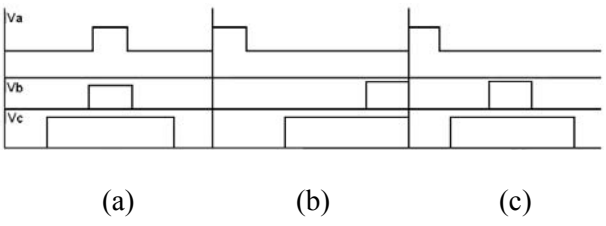


Figure 5. Pulse pattern for a three phase inverter: (a) the centering pulse pattern, (b) one of the 27 pulse pattern combinations, and (c) optimum pulse pattern with centering and low common mode voltage.

voltage (same as the one in Figure 4b) but generates a better load current. In fact, cases (b) and (c) have similar CMV values but do not have similar load currents.

The controller randomly selects one of the optimum pulse patterns. This is another advantage of the proposed method which spreads the spectrum contents of the output voltage; results in a low electromagnetic interference and mechanical vibration.

3. SIMULATION RESULTS

To evaluate performance of the proposed technique, it was simulated using the Matlab software. The circuit was simulated using a three-phase three-level flying capacitor inverter with an inductive-resistive load, and the parameters were chosen as below: $R = 1\Omega$, $L = 23\ mH$, $C_a = C_b = C_c = 1mF$, $V_d = 1000\,v$. In the SVM technique, the modulation index (m) is defined as:

$$m = \frac{V_f}{V_d/2}$$

V_f is the fundamental voltage (inverter output) which must be constructed by using adjacent vectors. Figure 7 shows this voltage versus (m) in the whole linear modulation range.

Capacitors in the circuit are assumed to have $V_a = 800\,v$, $V_b = 300\,v$ and $V_c = 500\,v$ initial voltages to find how the controller can control these voltages. The results are compared to the results of the case that all pulses are at the center of the switching cycles. The simulation results are shown in Figures 8 and 9. In this performance comparison, the simulations have been carried out for three cycles (60 ms in total). As can be seen from the Figures 8 and 9, the capacitors voltages can be controlled properly. A numerical comparison has been done between the optimum and the conventional method. The conclusions are shown in Table 3. In this comparison, the number of the CMV levels, the number of dv/dt in branch voltages in one switching cycle and the number of dv/dt in the CMV in one switching cycle in both methods has been compared. The numbers shows the advantages of the novel method clearly. Also it can be seen that the CMV in the novel method has less dv/dt than the CMV in conventional method which has the advantage of less common-mode electromagnetic interference (EMI) emission. It can be seen from Figure 9 that the proposed technique has many advantages over the conventional technique in reducing the common-mode voltage. In this method, the common mode voltage is decreased from five levels (in conventional method) down to three levels for the same switching losses while the capacitors voltages are controlled.

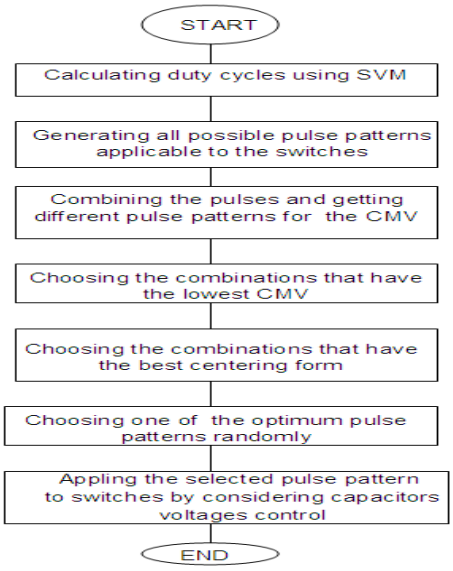


Figure 6. Algorithm of the novel method.

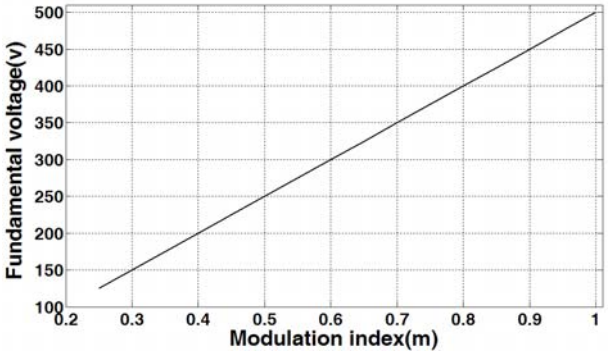
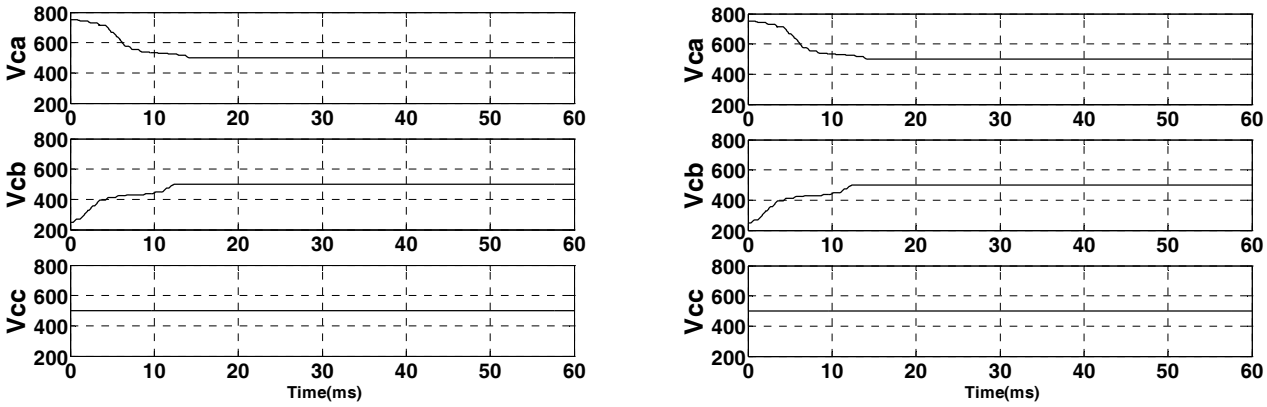
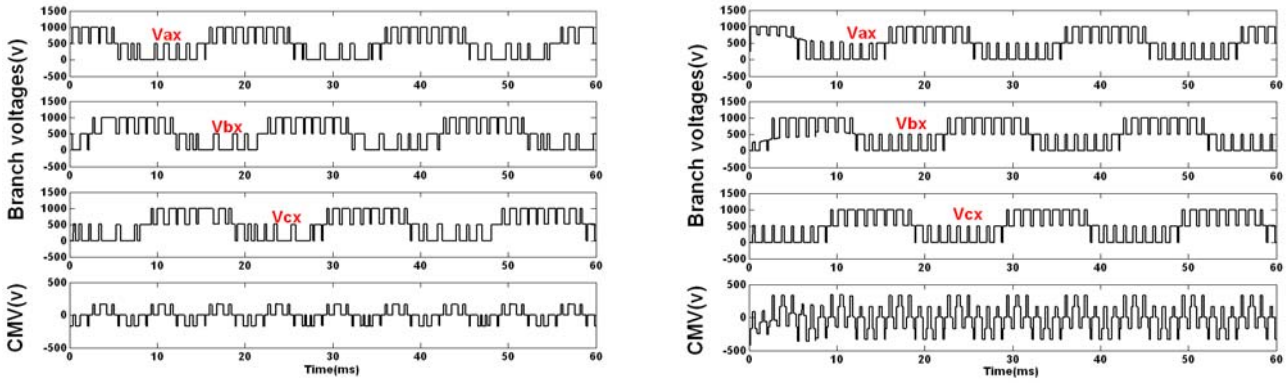


Figure 7. Fundamental voltage versus (m) in the whole linear modulation range.



(a) (b)

Figure 8. Capacitors voltages (a) novel method (b) conventional method.



(a) (b)

Figure 9. Leg voltages and CMV for a three-phase three-level inverter with inductive-resistive load (a) novel method (b) conventional method (all of the pulses are centered).

TABLE 3. The Numerical Comparison Between the Conventional and the Novel Method.

Comparison Subject / Method	The number of CMV levels in one cycle	The number of dv/dt in Vcx in one switching cycle	The number of dv/dt in Vbx in one switching cycle	The number of dv/dt in Vax in one switching cycle	The number of dv/dt in the CMV in one switching cycle
Conventional Method	5	38	38	38	100
Novel Method	3	35	35	35	81

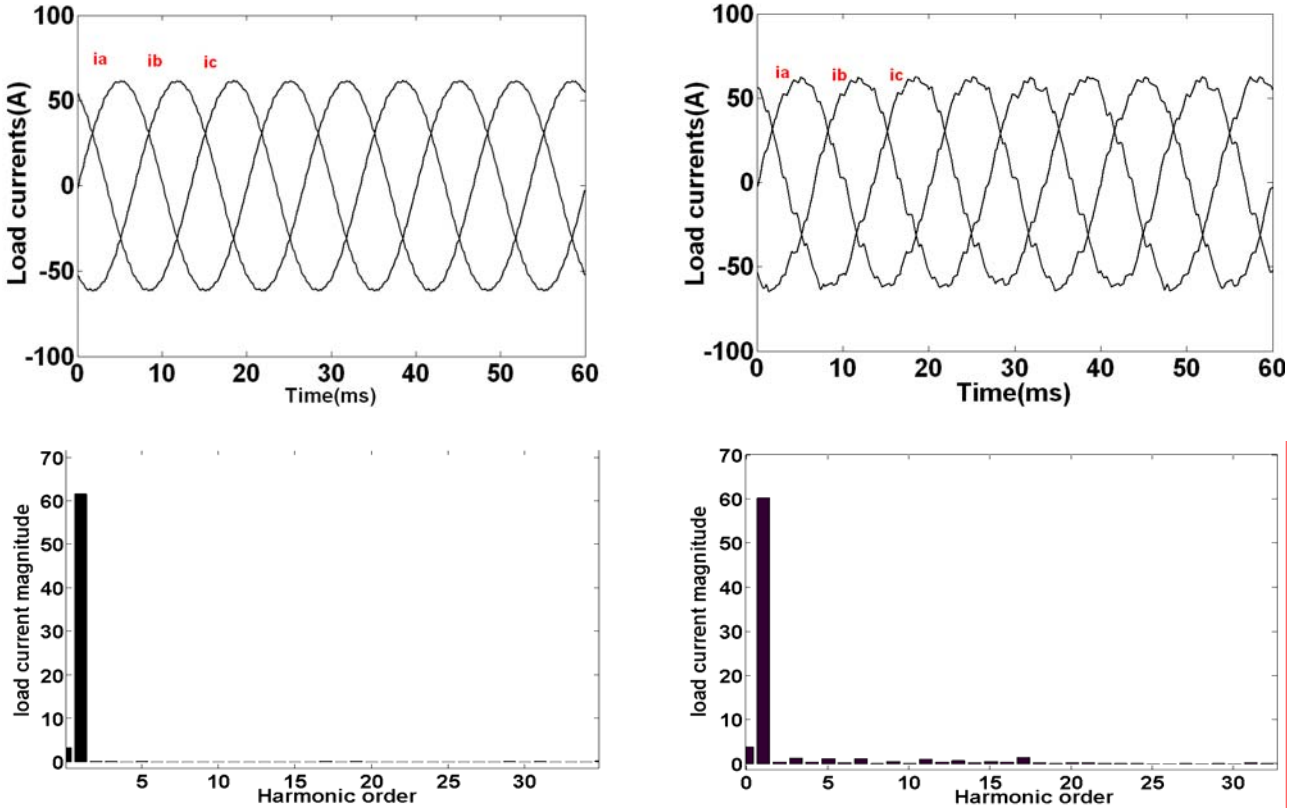


Figure 10. Load current and its harmonic spectrum in a three-phase three-level inverter (a) conventional method, (b) novel method.

The load current and its harmonic spectrum, in both conventional and novel methods, have also been shown for one cycle in Figure 10. As can be seen, there is no considerable difference between the harmonic spectrums of the two methods. A total harmonic distortion (THD) calculation has been done to prove this claim. As a fixed pulse pattern is not used in the novel method and the selection of the final pattern is based on a random selection, so the THD does not have a determined value. The true THD value can be obtained by averaging THD values in several different cycles. Table 4 shows the THD comparison results of the proposed method versus conventional method in the whole linear modulation range. The graph of this comparison has also been shown in Figure 11. In fact, CMV reduction increases the current THD but the novel method proposed here, keeps the best possible.

As it was mentioned before, the proposed technique can be applied to more than three voltage levels without significantly changing the control circuit. The simulation results on a five-level inverter have also been shown in Figures 12-14 to further support this claim. The reduction techniques for three-level and five-level inverters are the same. The only difference is that a five-level inverter with the flying capacitor topology has three capacitors in each leg. On the other hand, there are 9 capacitors in a three-phase five-level inverter that their different charge and discharge states must be considered according to load current. In each leg, the capacitors initial values must be 250, 500 and 750 volts. But these values are assumed to be 200, 500 and 800 respectively in order to show the controllability of this method. A three-phase five-level inverter has twelve levels of common-mode voltage while it is reduced to 3

TABLE 4. The THD Comparison Between Conventional and Novel Method in the Whole Linear Modulation Range.

m	Conventional Method THD	Novel Method THD
0.25	5.19	16.31
0.3	5.05	14.75
0.35	4.83	13.53
0.4	4.32	13.02
0.45	3.93	11.28
0.5	3.8	11.01
0.55	3.75	10.56
0.6	3.43	9.67
0.65	3.59	8.8
0.7	3.6	7.75
0.75	3.66	7.01
0.8	3.37	6.32
0.85	3.34	5.86
0.9	3.41	5.36
0.95	3.39	4.25
1	3.43	3.64

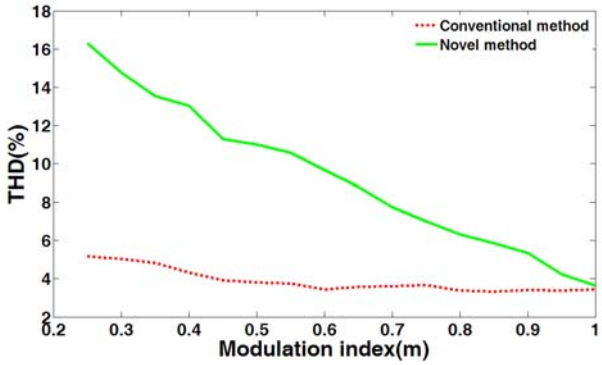
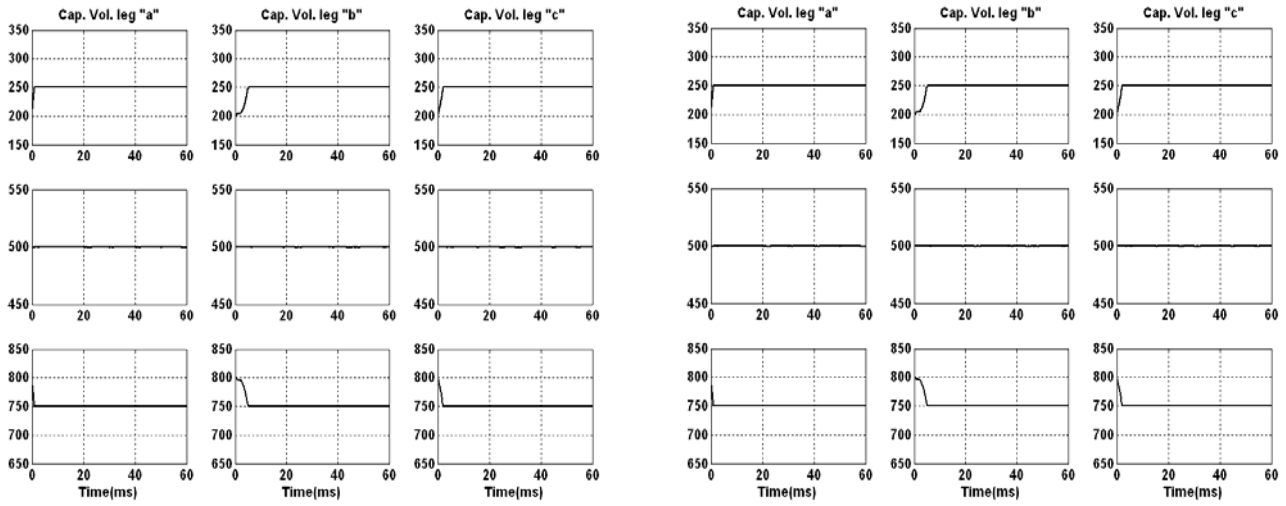


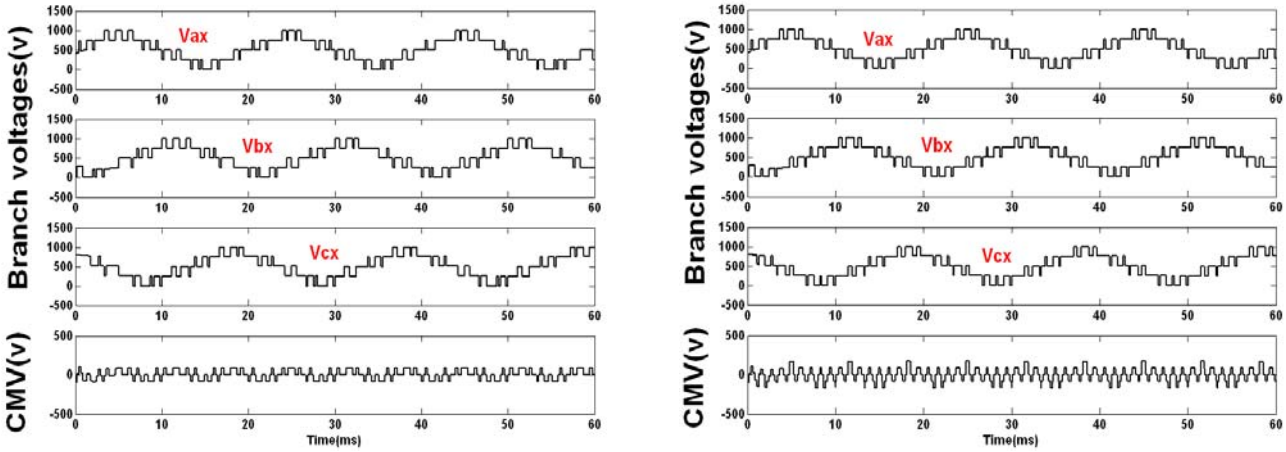
Figure 11. Graph of the THD comparison between conventional and novel method in the whole linear modulation range.

levels in the proposed method. The load current and its harmonic spectrum, in both conventional and novel methods, have also been shown for one cycle in Figure 14. In a real case, the proposed method can be implemented by a random PWM generator which is controlled by a microcontroller. We expect the proposed method to have less CMV with respect to conventional method.



(a) (b)

Figure 12. Capacitors voltages (a) novel method (b) conventional method.

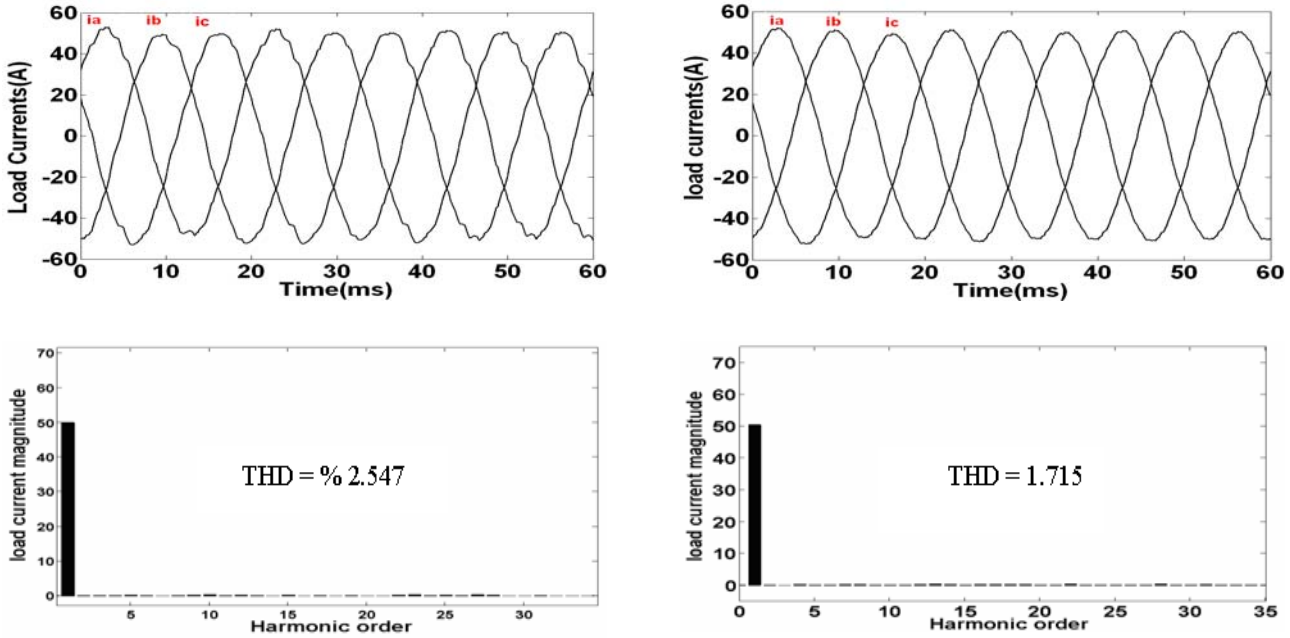


(a) (b)

Figure 13. Leg voltages and CMV for a three-phase three-level inverter with inductive-resistive load (a) novel method (b) conventional method (all of the pulses are centered).

4. CONCLUSIONS

Multilevel voltage source inverters are a new generation of inverters. They are suitable for high power and high voltage applications due to reduced harmonic contents and low voltage stress. Multilevel inverters have different voltage levels and switching states. They may reduce and control the CMV which assists the generation of a high quality (low harmonic) voltage and current. In this paper, a novel CMV reduction and control technique is proposed for a three-phase multilevel inverter which controls the capacitors voltages and load currents with low switching losses. The



(a) (b)

Figure 14. Load current and its harmonic spectrum in a three-phase five-level inverter (a) novel method, (b) conventional method.

controller selects one of the optimum pulse patterns (with low CMV) randomly which has another advantage of spreading the spectrum contents of the output voltage for low electromagnetic interferences and mechanical vibration. Finally one other advantage of this method is that the technique can be applied to more than three voltage levels without a significant change in the control circuit.

5. REFERENCES

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