RESEARCH NOTE

GENERATION OF THREE-PHASE PWM INVERTER USING XILINX FPGA AND ITS APPLICATION FOR UTILITY CONNECTED PV SYSTEM

S. Mekhilef and N. A. Rahim

Power Electronics Research Laboratory, Department of Electrical Engineering
University of Malaya, 50603 Kuala Lumpur, Malaysia, saad@um.edu.my

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Abstract Analysis and practical implementation of the regular symmetric sampled three-phase PWM inverter waveform has been presented in this paper. It is digitally implemented on a Xilinx field programmable gate array FPGA, and the essential considerations involved in the feasibility of using a Xilinx XC4008E software-based to generate PWM has been discussed. All the necessary Xilinx hardware/software techniques and programs required to implement and generate three-phase Pulse Width Modulation (PWM) are developed in detail, and demonstrated using practical results from an experimental Xilinx board. The techniques developed and presented in this paper are readily applicable to other currently available Xilinx chips. Simulation and experimental results of grid-connected inverter are presented. From the simulation and experimental results it is confirmed that the harmonic distortion of the output current waveform of the inverter fed to the grid is within the stipulated limits laid down by the utility companies.

Key Words Pulse Width Modulation (PWM), FPGA, Inverter, Photovoltaic (PV)

چکیده تحلیل علمی و کاربرد عملی نمونه مبدل شکل موج PWM نوع سه فاز متقارن معمولی در این مقاله ارائه شده است. کاربرد این وسیله به فرم دیجیتال بر آرایه قابل برنامه ریزی FPGA با میدان زیلینکس Xilinx تجربه گردیده و امکان بکارگیری برنامه نرم افزاری Xilinx XC4008E برای تولید PWM بررسی شده است. همهٔ فناوری های سخت افزاری و نرم افزاری ضروری زیلینکس و برنامه های لازم برای بکارگیری و تولید مدول سه فاز با پهنای پالسی PWM به تفصیل توسعه یافته و با استفاده از نتایج عملی حاصل از یک نمونه زیلینکس آزمایشی ارائه شده است. روش های توسعه یافته مورد بحث در این مقاله برای سایر چیپ های معمولی نوع زیلینکس نیز به سادگی قابل اعمال است. نتایج شبیه سازی و تجربی مبدل های مشبک متصل نیز در این مقاله ارائه شده است. نتایج تحقیق نشان داد که اعوجاج هارمونیک جریان موج خروجی مبدل تغذیه شده به داخل صفحه مشبک در حد قابل قبول شرکت های کاربر قرار داشت.

1. INTRODUCTION

The heart of any PWM control scheme is undoubtedly the switching strategy used to generate the switching edges of the PWM control waveform [1]. It is possible, by surveying the literature over the last decade to trace the historical development of PWM switching techniques and relate these developments to changes in technology, starting from analogue-based systems through discrete digital, and more recently ROM-based and microprocessor-implemented controls schemes [2].

Most analogue implemented PWM-control schemes have been based upon “natural” sampled switching strategies [3]. More recently, a new switching strategy referred to as “regular sampling”, has been proposed which is considered to have a number of advantages when implemented using digital techniques [2]. Since both natural and regular sampling techniques can be implemented using microprocessor technology, and are therefore likely to form the basis of most microprocessor based PWM control.

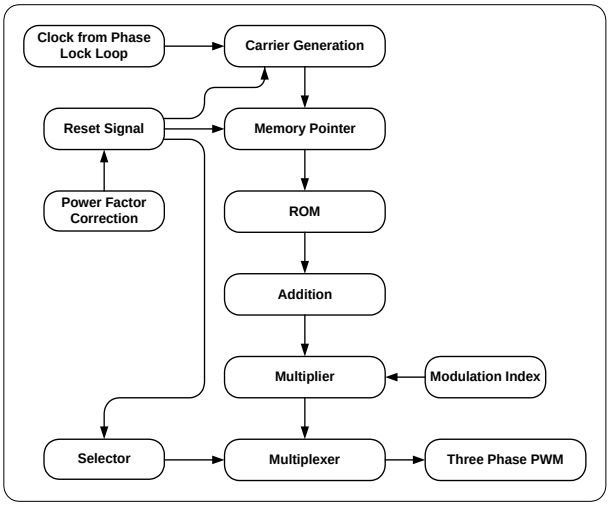

Figure 1. Block diagram PWM generator using Xilinx FPGA

2. PWM GENERATOR USING XILINX FPGA

FPGA is Programmable Logic Device developed by Xilinx, Inc. It comprises of thousand of logic gates. Some of them combined together to form a Configurable Logic Block (CLB). CLB simplifies higher-level circuit design. Gates interconnections using software are defined through SRAM or ROM. This provides flexibility to modify the designed circuit without altering the hardware part. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low cost for a complex circuitry and rapid prototyping make it as the most favorable choice for prototyping an ASIC [5-7].

The overall block diagram of the three-phase PWM generator is shown in Figure 1. The carrier wave is compared with the multiplied modulating signal from the look-up table. The data of the look up table are stored in the internal ROM unit. The external multiplicand and the stored data will determine the modulation index of the PWM.

The data stored in the look-up table (ROM) consists of 60 data from the Red phase and another 60 data from the Blue phase. Part of Yellow phase is derived using addition of Red and Blue phases. Selector Unit and Multiplexer are used to select the required signal to the appropriate channel as to form a proper PWM output pattern at the output terminals.

The shifting of signal waveform is essential in order to vary the power factor of the system. This is carried out by delay or advance the reset signal. The reset signal is tied up to the entire module. A positive triggering edge during positive and negative cycle is used as a reference by the reset signal. Advancing or delaying the reset signal by the external command will force the current in the main circuit to lead or lag the voltage supply.

2.1 Generation Modulating Wave Sinusoidal modulating waves are commonly used in PWM schemes, although other types of modulating wave, such as trapezoidal or triangular waves, have been employed in certain applications. The generation of a sine wave using Xilinx FPGA was done by storing the sine values in a lookup table, which is pre-programmed into permanent memory (ROM) the values having first been calculated [8].

The memory requirement, efficiency of operation, and accuracy of the output waveform depends on the number of sample values defining a cycle of the sine wave and their resolution. If for example, the values are taken at 0.5^0 intervals, then a complete modulating cycle is defined by 720 values. The modulating wave could be defined at a greater number of sample points, but the memory requirement is proportionally increased. Hence, the point at which a sample is taken for the modulating process directly corresponds to a value in the lookup table. If a single-phase carrier is generated then each frequency ratio must be a multiple of three to eliminate the carrier frequency harmonics [9-10]. In this case 60^0 data are stored of two phase and the third is derived from.

2.1.1. Look-Up Table The sample of Red phase and Blue phase data, which are stored in the look-up table, are shown in below. The look-up tables are formed using the internal ROMs unit of Xilinx XC4008E.

```
; memfile COS.mem for LogiBLOX symbol rom1
; Created on Saturday, July 14, 2002 16:47:55
; Header Section
RADIX 10
DEPTH 256
WIDTH 8
DEFAULT 0
; Data Section
```

```
; Specifies data to be stored in different addresses
; e.g., DATA 0:A, 1:0
RADIX 10
DATA
22,22,21,21,21,21,20,20,20,20,19,19,19,18,18,18,17,17,
17,16,16,16,
15,15,15,14,14,14,13,13,12,12,12,11,11,10,10,10,9,9,8,
8,7,7,7,6,6,5,
5,4,4,4,3,3,2,2,1,1,0,0
; end of LogiBLOX memfile

; memfile SIN.mem for LogiBLOX symbol ROM1
; Created on Saturday, July 14, 2002 16:27:52
;
; Header Section
RADIX 10
DEPTH 256
WIDTH 8
DEFAULT 0
;
; Data Section
; Specifies data to be stored in different addresses
; e.g., DATA 0:A, 1:0
RADIX 10
DATA
0,0,1,1,2,2,3,3,4,4,4,5,5,6,6,7,7,7,8,8,9,9,10,10,10,11,11
,12,12,12,
13,13,14,14,14,15,15,15,16,16,16,17,17,17,18,18,18,19,
19,19,20,20,
20,20,21,21,21,21,22,22,
; end of LogiBLOX memfile
```

2.2 Triangular Carrier Generation The triangular carrier wave can be generated using up/down counter. The rate at which this counter is incremented (or decremented) determines the carrier frequency and accuracy of the sampling process. Each time the counter is incremented (or decremented), its output is compared with a sampled value of the modulating wave to determine the switching edge of the PWM waveform.

2.2.1 Carrier Frequency Determination Determination of carrier frequency is the first step of design process, where the clock frequency needs to be calculated precisely. The carrier frequency (f_c) had been decided to operate at 18 kHz. The decision was based on various factors such as inverter topology, acoustic radiation, type of power switching devices used and limitation of the peripheral components. Operating at high frequency is better than the low frequency where the harmonic components could be shifted to high order. However at high frequency more switching stress and power losses occur in the devices especially in the three devices controlled bridge topology.

The carrier frequency has a relationship with the main clock frequency and the up-down counter that could be expressed as:

$$f_c = f_{clk}/[2(2^n - 1)] \quad (1)$$

Where f_c is the carrier frequency, f_{clk} is the main clock frequency and n is the bit size of the up-down counter.

2.2.2. Determination of Main Clock Signal An 8-bit up-down counter must be clocked at 9.18MHz to produce 18kHz carrier frequency according to Equation 1. The clock signal is locked and synchronized with the AC mains frequency of 50Hz by using an external phase-locked loop circuitry. The division of clock frequency from 9.18MHz to 50Hz is accomplished by using internal counter in the Xilinx chip. The 50Hz feedback frequency is used as an input to the phase-locked loop (PLL) chip to lock the phase with the supply phase reference voltage.

3. INVERTER CONFIGURATION

Figure 2 shows the schematic description of a PV utility-interactive system. The power Inverter is primarily responsible for converting the DC PV power into utility compatible AC power and for synchronizing and transferring that AC power safely into the utility grid.

The DC power available at the output of the PV array is converted to AC power using Pulse width modulated (PWM) inverter generated using FPGA Xilinx. The PWM signal used to switch the power IGBT's. The inverter under consideration is capable of minimizing the level of the harmonic content of the load current waveform. It should not be susceptible to the load variations and therefore its overall performance must be superior over conventional type of PWM inverter.

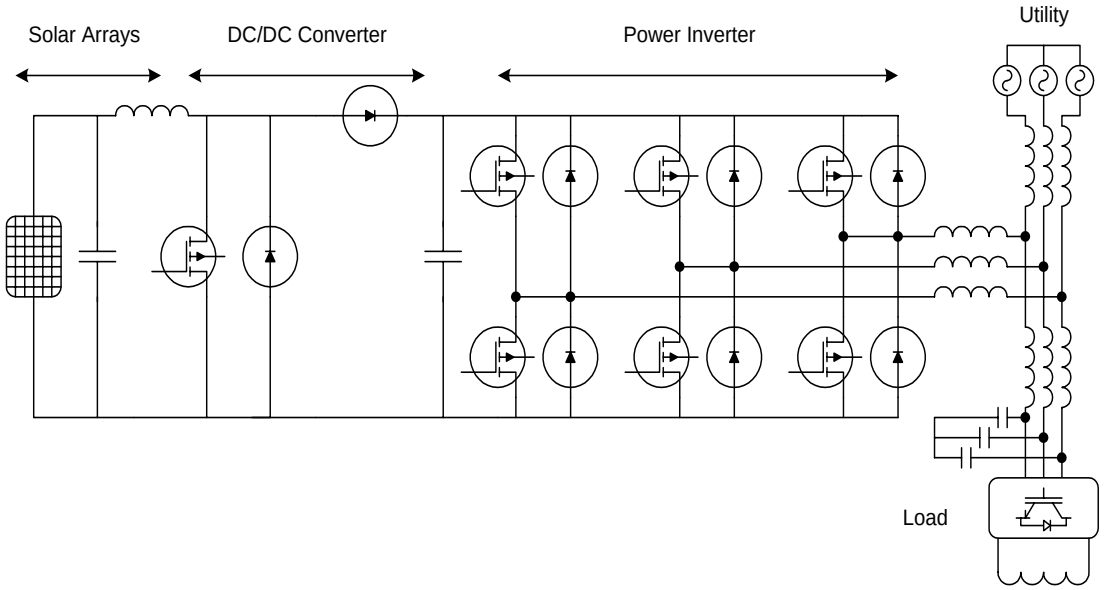

Figure 2. Proposed Photovoltaic utility-interactive system scheme.

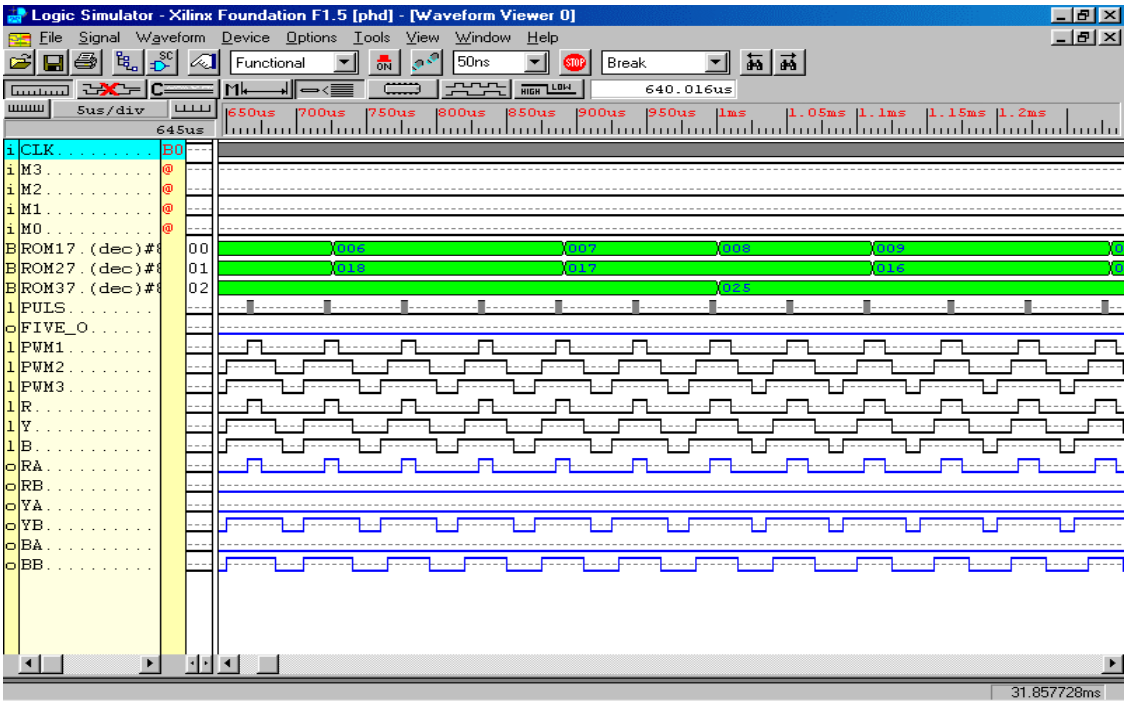

Figure 3. Three-phase PWM simulation Results using Xilinx.

4. RESULTS

The selected results have been chosen to illustrate some of the main features of the new three-phase Pulse Width Modulation (PWM) generated using Xilinx XC4008E. Simulation is performed using

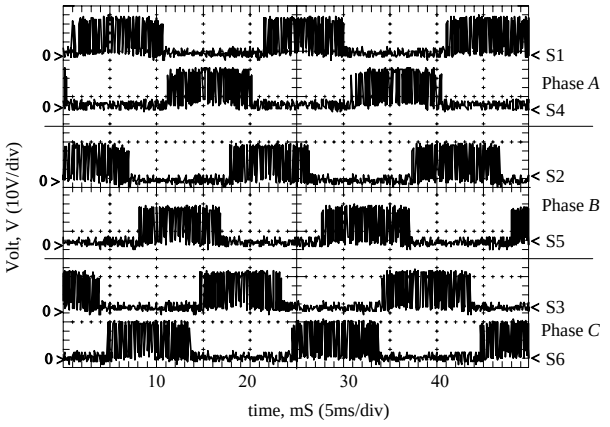

Figure 4. Three-phase PWM generated using XC4008E.

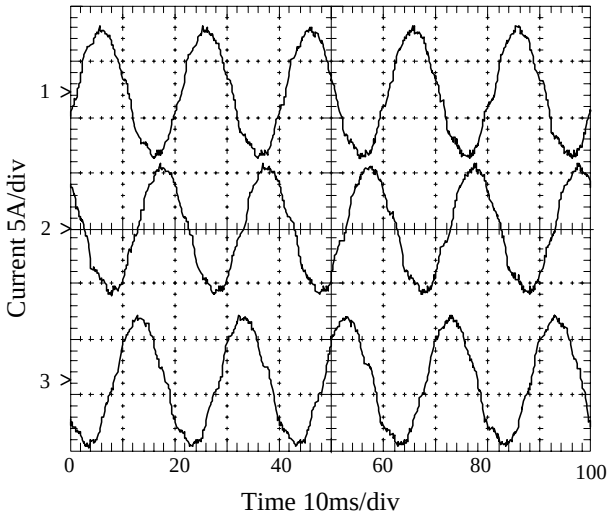

Figure 5. Three-phase output current of the inverter.

the 1.5 foundation series in Figure 3 the simulation of three-phase PWM inverter is shown applied to the six switches of the inverter scheme whereas Figure 4 shows the six PWM waveforms generated using Xilinx XC4008E each one is applied to one IGBT in the power circuit. Figure 5 shows the three-phase output current of the inverter using low pass filter.

5. CONCLUSION

Using Xilinx FPGA to generate the PWM provides flexibility to modify the designed circuit without altering the hardware part. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low cost for a complex circuitry and rapid prototyping make it as the most favorable choice for the PWM generation. From the simulation and experimental results it is confirmed that the harmonic distortion of the output current waveform of the inverter fed to the grid is within the stipulated limits laid down by the utility companies, the THD is less than 5%. All the above advantages have made the inverter configuration highly suitable for grid connected photovoltaic application (5kW).

6. REFERENCES

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