DYNAMIC COMPENSATION OF ELECTRICAL POWER SYSTEMS USING MULTILEVEL VOLTAGE SOURCE INVERTER

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Abstract A New Static Var Generator (SVG), using cascaded full-bridge inverters (FBI) with binary output levels and the parallel connections of two cascaded inverters by means of current sharing reactor in each phases is introduced. The new M-level inverter, where M is 2^{n+2} - 3, consists of only 2n single-phase full bridges for each phases. The proposed technique not only increases the current capacity of proposed SVG but also decreases the output harmonic contents. Also, it can be connected directly to the distribution system without a transformer. Simulation results, based on the PSCAD/EMTDC, a high performance electromagnetic transient simulation program, are used to illustrate the flexibility of control action and also the performance of the proposed SVG in a power system environment.

Key Words Multi-Level VSI, Parallel Connection of VSIs, Harmonic Elimination, SVG

° °o®½BÇ¼pB–ñ¼¥Ç ¨¨Bª¼ °Bµo¼n±®½ª¬joŸ °ow ðªñ¼ »ñ½¼¼UBTwª Var k½k] k§±« ð½ ³§BŠ« -¼ª nj **²k¼ña** ¬C nj ³ÇŸ ³d†Çw M k½kÇ] ¤kLÇ« /Swª ²kÇ{ ³ÇªnA pBÇ- -¼Ç¼ u ¯o¼ ðªñ¼ ˜±- °ow ¤kL« °j ¬j±ª¯ °pª±« ¬ª±¼»« B´®¼ ³¯ °jB´®z½Q ¤kL« ðªŸ ³¼ ° ²j±¼ pB-o¼ nj pB–ñ¼¥Ç ¨¨Bª¼ o¼n±®½ª 2n ¥«B{ k{B¼»« M=2 $^{n+2}$ -3 -¼ÁBQ »¦¼i ¤kL« »]°oi Z±« ¥ñ{ »ñ¼±«nBµ °±Td« ³ñ¦¼ jo¼ ¿B¼ko¯Ç»]°oi rBT§° ° ¤kL« ¬B½o] S¼-o‹ -¼®`ªÇµ ° ¤kLÇ« ¤oT®ÇŸ ” B†íÇ¯ª S½¦¼BÇ› ° PSCAD/EMTDC n¼q–ª ¨¨o¯ ...w±¼ °pBw³¼L{ [½B¯ /j±¼ k¼µª± i /Swª ²k{ ²jª ¬Bz¯ Rnk› ·ñL{ ð½ ð¼«B®½j ¬±¼wªq¯BPªaŸ °ko¼ ¤kL« é½ow joñ¦ª¹î

INTRODUCTION

Modern high-tech industry needs reliable and high quality power supply. Undesirable supply quality can lead to an inadequate quality of products, interruption of important industrial precesses and therefore to economic losses. In addition, offices and consumers expect high supply quality to safeguard their equipment, which is sensitive to power quality. To minimize voltage fluctuations and imbalances, reactive power compensation is now widely used. It is also used to increase the power transmission capacity of ac lines. Fast and optimally controlled reactive power compensators improve the transient and small-signal stability of an inter-connected system as well as avoid voltage instability [1]. Fast control of reactive power compensators is made possible by the availability of semi-conductor switching devices. As new gate turn off devices have become energy efficient and available in larger power ratings, a new generation of Static Var Generators (SVG), Static Compensators (STATCOM), and Unified Power Flow Controllers (UPFC) are emerging in the market place [2,3,4].

SVGs, based on voltage source inverters employing gate-turn-off (GTO) thyristors, are showing promise of improving power factor and stabilizing transmission systems. An SVG can adjust the amplitude of the ac voltage, by means of pulse-width modulation (PWM) of the inverter or by controlling the dc bus voltage, thus injecting either a leading or lagging reactive power. A pulse-width-modulated SVG, in which the dc voltage is maintained constant, can respond rapidly to changing reactive power demand at the expense of increasing the switching and snubbing losses. Due to the rating restriction of the inverter switching devices, it is difficult to apply SVGs, using two or three-level inverters for high voltage and high power applications. To overcome this disadvantage, SVG systems using **multilevel inverters** have attracted tremendous intereset. The general structure of a multilevel inverter is to synthesize a sinusoidal voltage form several levels of voltages, typically obtained from capacitor voltages sources. As the number of levels increases, the synthesized staircase wave approaches the sinusoidal wave resulting in reduced harmonic distortion. The goal here is to minimize the harmonic distortion in the system, but at the same time the inverter scheme should be simple and compact. The different multilevel VSI schemes studied and tested so far include diode-clamp, flying-capacitor and cascaded separate dc source inverters [5,6].

To achieve a better waveform and also higher power ratings, in this paper, full-brige inverter units with binary output levels and the parallel connections of two cascaded inverters using a current sharing reactor in each phases is proposed. The new M-level inverter, where M is 2^{n+2}-3, consists of only 2n single-phase full bridges for each phase, e.g. with nÂ2, this inverter can generate almost sinusoidal voltage waveform with the least component count while retaining functional modularity. The switching timing angles are varied to control the fundamental output voltage and also to minimize waveform distortion, and are stored in the switching pattern table. This new multilevel inverter eliminates excessively large number of bulky transformers required by conventional multi-pulse inverters. It is suitable for flexible ac transmission systems (FACTS) applications including static var generation, power-line conditioning, series compensation, phase shifter, and voltage balancing because each dc capacitor voltage can be self-maintained and independently controlled without additional dc sources.

To illustrate the capabilities of proposed SVG for reactive power compensation, the detailed three phase transient simulation in 13.8 kV distribution system is carried out using PSCAD/EMTDC simulation program [7] for different operating conditions. This new converter topology can be easily adapted not only to reduce the dynamic distortion of power systems but also for other applications such as fuel cell and photovoltaic utility interface systems where the sources are originally isolated dc sources. Another possible application of this new converter is for adjustable speed drives requiring high efficiency, which may not be achievable with PWM techniques.

PROPOSED STATIC SYNCHRONOUS COMPENSATOR

The SVG for power system applications can be implemented by various, static switching converters, using semiconductor switching devices of suitable rating and characteristics. The synchronous SVG proposed in this paper is analogous to an ideal electromagnetic generator, it can produce a set of three alternating (almost sinusoidal) voltages at the desired fundamental frequency with controllable amplitude and phase angle. It can gernerate or absorb, reactive power when tied to an electric power system to function like a synchronous compensator without using any dc sources. It will be able also to exchange the active power

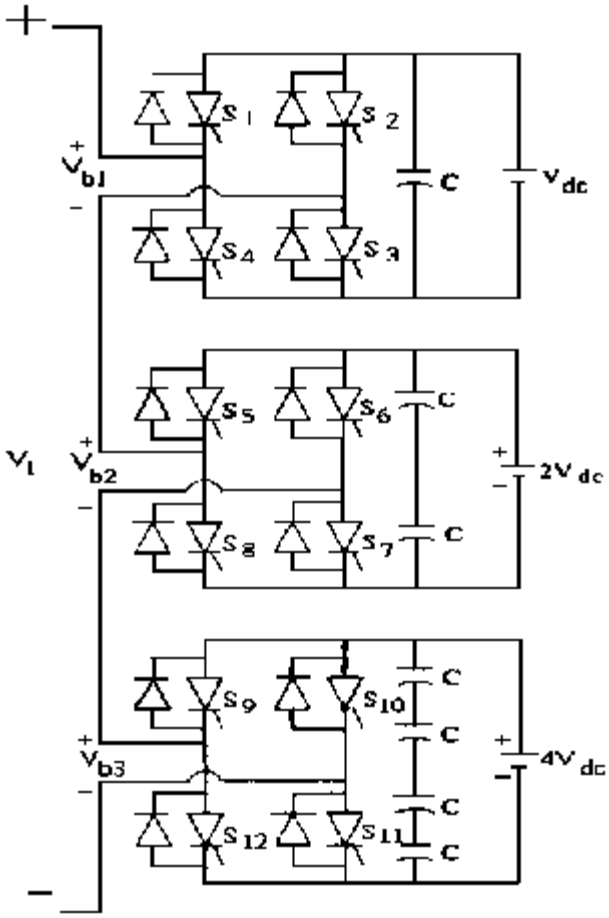

Figure 1. Proposed simple binary multilevel voltage.

between the ac system and a dc electric energy source storage, in other words with isolated dc sources in dc side of FBIs it is possible to use it also as a unified power flow controller (UPFC).

A. Structure and Principle of Operation of a Simple BMVSI Figure 1 shows the single-phase configuration of the proposed BMVSI. It consists of 3 Full-bridge inverter (FBI) units connected in cascade to generate a 2^{3+1}-1= 15 step output voltage over half fundamental cycle. Each FBI has its own dc source i.e. V_{dc}, $2V_{dc}$ and $4V_{dc}$ this new BMVSI does not require any transformers, clamping diodes, or flying capacitors and its advantage is that by using only 3 FBI units in each phases a 15-level approximately sinusoidal and fully

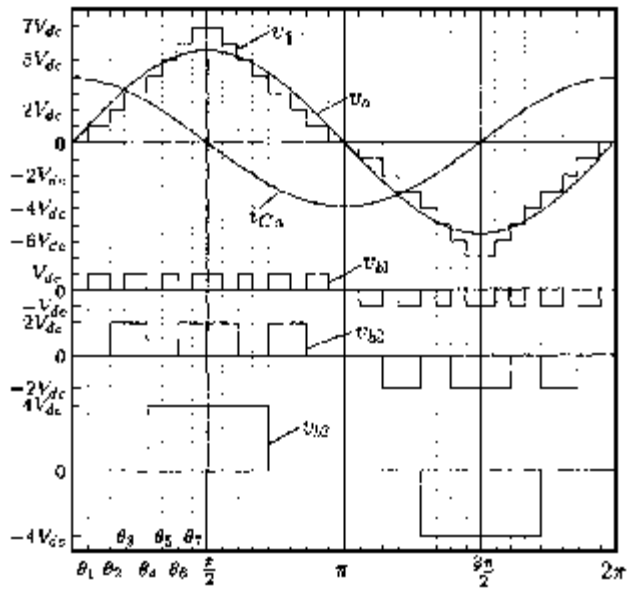

Figure 2. Generated waveforms by single-phase source inverter (BMVSI) topology. BMVSI in its ac side.

controllable output voltage is achieved [8]. Figure 2 shows waveforms generated by each FBI and also the output voltage u_1. It is the sum of 3 inverter unit output voltages, i.e. u_{b1}, u_{b2} and u_{b3}:

$$u_1 = u_{b1} + u_{b2} + u_{b3} \quad (1)$$

Each FBI unit generates three-level output, e.g. FBI- 1 generates+ V_{dc}, 0 and - V_{dc} which is made possible by connecting the dc-source sequentially to the ac side via the switching devices s_1, s_2, s_3 and s_4. The diodes and GTOs form a switching group which is bi-directional in current and uni-directional in voltage.

Table 1 lists 15 levels of the output voltages and their corresponding switch states for single-phase configuration of Figure 1 over one half fundamental cycle. State condition 0 means that the switch is off and 1 means that the switch is on. As seen in this Table the total number of switchings of FBI-1, FBI-2 and FBI-3 for each half cycle is 4, 2 and only 1 respectively. The waveform of u_1, illustrated in Figure 2 contains odd harmonics of the fundamental waveform i.e.:

TABLE 1. Fifteen Levels of the Output Voltage and Their Corresponding Switch States for Single-phase Configuration of BMVSI Over an Half Fundamental Cycle.

n_1 =	Switch states											
	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	s_9	s_{10}	s_{11}	s_{12}
$7V_{dc}$	1	0	1	0	1	0	1	0	1	0	1	0
$6V_{dc}$	1	1	0	0	1	0	1	0	1	0	1	0
$5V_{dc}$	1	0	1	0	1	1	0	0	1	0	1	0
$4V_{dc}$	1	1	0	0	1	1	0	0	1	0	1	0
$3V_{dc}$	1	0	1	0	1	0	1	0	1	1	0	0
$2V_{dc}$	1	1	0	0	1	0	1	0	1	1	0	0
V_{dc}	1	0	1	0	1	1	0	0	1	1	0	0
0	1	1	0	0	1	1	0	0	1	1	0	0
$-V_{dc}$	0	1	0	1	1	1	0	0	1	1	0	0
$-2V_{dc}$	1	1	0	0	0	1	0	1	1	1	0	0
$-3V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
$-4V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
$-5V_{dc}$	0	1	0	1	1	1	0	0	0	1	0	1
$-6V_{dc}$	1	1	0	0	0	1	0	1	0	1	0	1
$-7V_{dc}$	0	1	0	1	0	1	0	1	0	1	0	1

$$u_1 = \sum_{k=1} V_{2k-1} \sin[(2k-1)\omega t] \quad (2)$$

where V_{2k-1} is the amplitude of (2k-1)th output harmonic (k = 1,2,3,...):

$$V_{2k-1} = \frac{4}{(2k-1)\pi} \sum_{i=1}^{N} V_{dc} \cos[(2k-1)\theta_i] \quad (3)$$

with $N = 2^n - 1$, in a 15-level BMVSI, n = 3 and N = 7. The switching timing angles θ_i (i=1,2,3,...,7) for this 15-level BMVSI, are to be calculated off-line to eliminate some lower order harmonics for a given modulation index (MI), which is defined as $\frac{V_1}{V_{1max}}$, where V_1 is the amplitude of the fundamental component of the BMVSI output phase voltage:

$$V_1 = \frac{4}{\pi} \sum_{i=1}^{7} V_{dc} \cos(\theta_i) \quad (4)$$

TABLE 2. The Switching Timing Angle Control of BMVSI for Different Values of MI = V_1/V_{1max}.

MI =	Switching angles						
	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7
0.510	25.88	40.55	48.86	56.12	65.06	74.15	89.08
0.550	20.23	33.81	47.46	54.7	62.22	70.19	89.26
0.600	14.29	33.54	39.02	52.35	66.71	58.82	84.47
0.680	16.10	23.72	35.19	50.34	54.22	62.67	67.40
0.700	13.51	22.02	31.56	45.25	57.06	58.47	67.81
0.730	9.54	20.07	26.70	39.37	52.34	58.38	67.49
0.750	6.84	18.28	24.46	35.58	48.50	56.97	67.89
0.770	3.37	15.55	23.12	32.06	44.56	53.64	69.16
0.800	7.22	13.07	20.85	27.75	39.13	54.53	62.72
0.810	5.42	13.32	19.31	27.05	37.09	51.92	63.09

V_{1max} is the maximum obtainable amplitude i.e. the amplitude of the phase voltage when all switching angles θ_i are equal to zero, from Equation 4 it becomes: $V_{1max} = \frac{4}{\pi}(7V_{dc}) = 8.9127V_{dc}$.

The angles θ_i can be varied to control the fundamental output voltage of the BNVSI, and also minimize the distortion, for 15 level VSI in three-phase system 5th, 7th, 11th, 13th, 17th and 19th output voltage harmonics can be chosen. The switching timing angles θ_i (i= 1,2,...7) are calculated to eliminate above mentioned harmonics for different values of MI, and stored in a switching pattern table as shown for some vlues of MI in Table 2.

B. Structure and Principle of Operation of Parrallel BMVSI Figure 3 shows the single-phase configuration of the proposed parallel connection of two binary multi-level VSI (BMVSI) by means of a current sharing reactor L. Each BMVSI consist of n FBI units connected in cascade to generate a $2^{n+1} - 1$ step output voltage over half fundamental cycle [9], e.g. in this figure n=2 and therefore the output

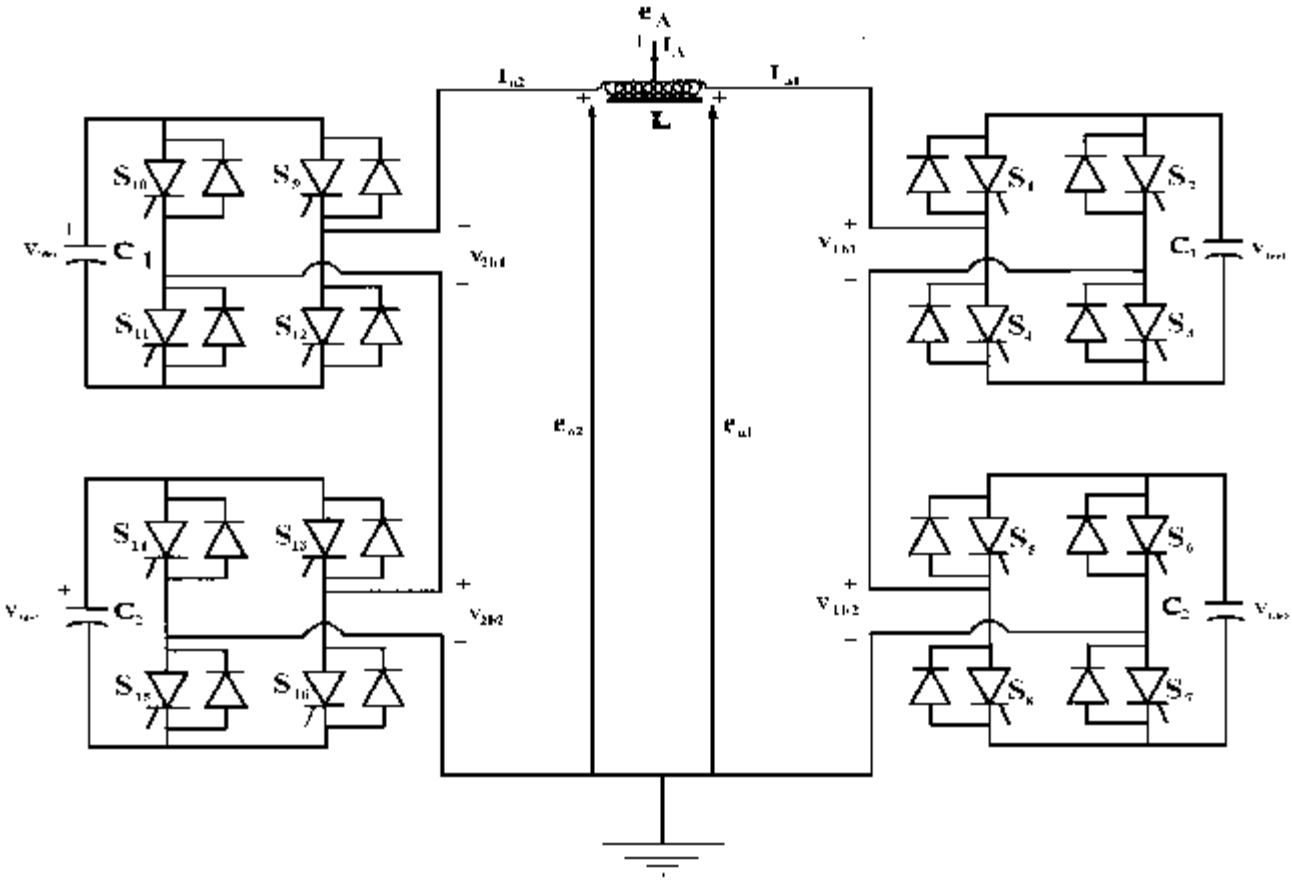

Figure 3. Proposed binary multilevel voltage source inverter (BMVSI) topolagy.

voltage of each BMVSI has 2^{2+1}-1= 7 step output voltage over half fundamental cycle. By means of this configuration the output voltage of phasee A, i.e. e_A and its current, i.e. i_A become respectively:

$$e_A = \frac{e_{a1} + e_{a2}}{2} \quad (5)$$

$$i_A = i_{a1} + i_{a2} \quad (6)$$

where e_{a1}, e_{a2}, i_{a1} and i_{a2} are respectively the output voltages and currents of each BMVSI in phases A. e_{a1} and e_{a2} are the sum of corresponding cascaded n FBI unit output voltages, i.e.:

$$e_{al} = \sum_{k=1}^{n} V_{1bk} \quad (7)$$

$$e_{a2} = \sum_{k=1}^{n} V_{2bk} \quad (8)$$

where V_{1bk} and V_{2bk} are output voltages of FBIs and depending switching strategy of FBIs, their values in general case will be + $2^{k-1}V_{dc}$, 0, -$2^{k-1}V_{dc}$ and for Figure 3 as n=2: + V_{dc}, 0, + V_{dc} or + $2V_{dc}$, 0, -$2V_{dc}$. By appropriately turning on and off of different switching devices as illustrated in Figure 4(c) and Figure 4(f) e_{al} and e_{a2} become 7 step output voltages, therefore from Equation 5, e_A becomes $2(2^3-1)$ -1 = 13 steps output voltage as it is seen in Figure 4(g) along with its fundamental component (in general case e_A is $2(2^{n+1}-1)-1=2^{n+2}-3$ steps output voltage). With reference to Figure 3, the current sharing reactor consists of two magnetically 0.5 mH coupled inductors that equalize the instantaneous currents i_{a1} and i_{a2} [9]. e.g. if the current i_{a1} tends to increase over the current i_{a2}, a counter emf is induced in proportion to the

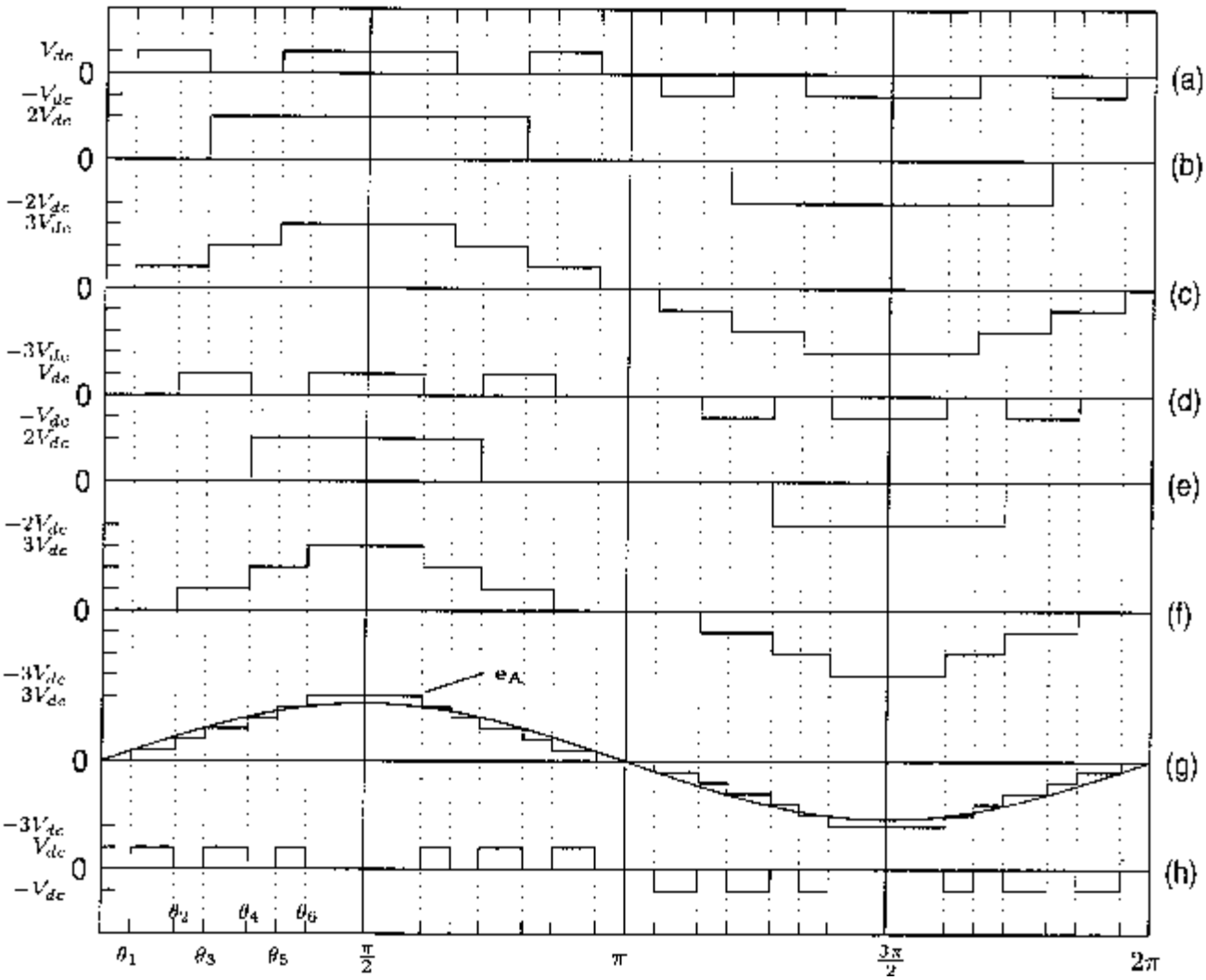

Figure 4. Typical output wave forms for proposed configuration of SVG: (a)-The voltage V_{1b1}. (b)-The voltage V_{1b2}. (c)-The voltage e_{a1}. (d)-The voltage V_{2b1}. (e)-The voltage V_{2b2}. (f)-The voltage e_{a2}. (g)-The voltage e_A and its fundamental component. (h)-The voltage across the current sharing inductor L.

unbalanced current which makes current i_{a1} decrease and i_{a2} increase. At the time when current i_{a1} and i_{a2} are balanced, no emf in the windings of the reactor is generated. Therefore, each side of the reactor carries half of the line current of the SVG. Figure 4(h) shows the voltage across the pole terminals of the sharing inductor L. Table 3 lists 13 levels of the output voltages e_A and their corresponding switch states for single-phase configuration of Figure 3 over one half fundamental cycle. The waveform of e_A, illustrated in Figure 4(g) contains odd harmonics of the fundamental waveform i.e.:

$$e_A = \sum_{k=1}^{\infty} E_{2k-1} \sin[(2k-1)\,wt] \qquad (9)$$

where E_{2k-1} is the amplitude of (2k-1)th output harmonic (k =1, 2, 3, ...):

$$E_{2k-1} = \frac{2V_{dc}}{(2k-1)\,p} \sum_{i=1}^{N} \cos[(2k-1)\,q_i] \qquad (10)$$

with $N= 2^{n+1}-2$, in a 13-level SVG, n= 2 and N= 6. The switching timing angles q_i(i= 1, 2, .., 6) for this 13-level SVG, are to be calculated off-line to eliminate some lower order harmonics i.e. N-1 non-triple odd harmonics of order 6m×1 for a given modulation index MI

TABLE 3. Thirteen Levels of the Output Voltage and their Corresponding Switch States for Single-Phase Configuration of SVG Over a Half Fundamental Cycle.

Phase-A	$e_A = \frac{e_{a1}+e_{a2}}{2} = \frac{1}{2} kV_{dc}$												
k	6	5	4	3	2	1	0	-1	-2	-3	-4	-5	-6
S_1	1	1	1	1	1	1	1	0	0	1	1	0	0
S_2	0	0	1	1	0	0	1	1	1	1	1	1	1
S_3	1	1	0	0	1	1	0	0	0	0	0	0	0
S_4	0	0	0	0	0	0	0	1	1	0	0	1	1
S_5	1	1	1	1	1	1	1	1	1	0	0	0	0
S_6	0	0	0	0	1	1	1	1	1	1	1	1	1
S_7	1	1	1	1	0	0	0	0	0	0	0	0	0
S_8	0	0	0	0	0	0	0	0	0	1	1	1	1
S_9	1	1	1	1	1	1	1	1	0	0	1	1	0
S_{10}	0	1	1	0	0	1	1	1	1	1	1	1	1
S_{11}	1	0	0	1	1	0	0	0	0	0	0	0	0
S_{12}	0	0	0	0	0	0	0	0	1	1	0	0	1
S_{13}	1	1	1	1	1	1	1	1	1	1	0	0	0
S_{14}	0	0	0	1	1	1	1	1	1	1	1	1	1
S_{15}	1	1	1	0	0	0	0	0	0	0	0	0	0
S_{16}	0	0	0	0	0	0	0	0	0	0	1	1	1

$= \frac{E_1}{E_{1max}}$, where E_1 is the amplitude of the fundamental component of the SVG output phase voltage:

$$E_1 = \frac{2V_{dc}}{p} \sum_{i=1}^{6} \cos(q_i) \qquad (11)$$

E_{1max} is the maximum obtainable amplitude i.e. the amplitude of the phase voltage when all switching angles q_i are equal to zero, from Equation 11 it becomes: $E_{1max} = \frac{12}{p} V_{dc}$.

The angles q_i can be varied to control the fundamental output voltage of the SVG, and also minimize the distortion. For 13 level in three-phase system 5th, 7th, 11th, 13th, 17th output voltage harmonics can be chosen.

To generate required reactive power from SVG, modulation index MI is varied and switching timing angles q_i(i= 1, 2, ..., 6) are calculated for each MI value. Due to nonlinear and transcendental characteristics, for each given MI, Equation 10 has to be numerically solved for switching angles q_i and great attention must be paid to the initial values of q_i using Newton-Raphson numerical technique. Using suitable inital conditions the solution for above mentioned equations for possible modulation index varying from 0.515 to 0.851 in steps of 0.001 are obtained and the results are illustrated in Figure 5. It is seen in this figure that for some values of MI instead of harmonic elimination only harmonic minimization is possible, i.e. MI= 0.63 and 0.76. When MI= 0.851 the SVG generates rated capacitive reactive power and when MI= 0.515 it absorbs rated inductive power. From Figure 5 it is seen that switching angles q_i are minimume for $MI = MI_{max}$, therefore these q_i are used to calculate capacitance values. The SVG current i_A either leads or lags the phase voltage e_A by $\frac{p}{2}$, therefore the average charge to each dc capacitor over every half cycle is equal to zero and because of this symmetric charge flow, voltages on all the dc capacitors remain theoritcally balanced.

However, because of the power losses in the SVG, capacitor voltages drift away from their set levels. In case of the BMVSI in Figure 3, the set voltage levels are V_{dc} and $2V_{dc}$. In principle, the charge and hence the voltage across each capacitor is maintained by prolonging or shortening the current flow through it. This is achieved by shifting the switching patterns. The direction of phase shift depends upon whether the inverter is producing leading vars or absorbing lagging vars.

MODELING AND SIMULATION RESULTS

Figure 6 shows the star connection of the three-phase structure of the proposed cascade

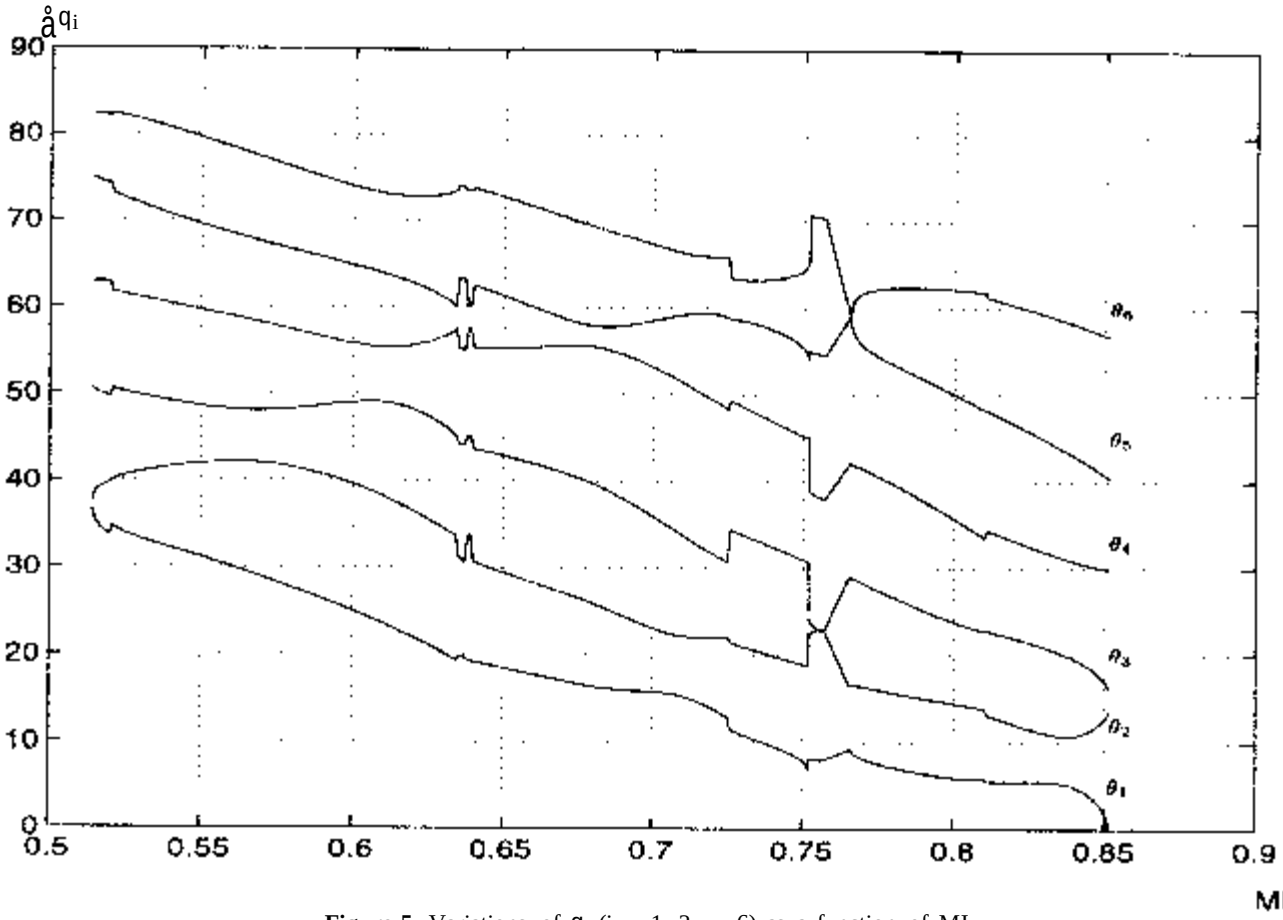

Figure 5. Variations of q_i (i = 1, 2, ..., 6) as a function of MI.

BMVSI seen in Figure 1. This configuration is used for the test system to illustrate three-phase simulation results.

The three-phase, 15-level VSI of Figure 6 is connected via a coupling transformer to an ac system as shown in Figure 7. For example, consider the total impedance on the ac side of 13.8kV to be 20% with 100MVA short circuit level, the dc side is rated with V_{dc}=1.732kV, i.e. 1.732, 3.464 and 6.928kV to support 3 FBIs in each phases. Using the switching pattern shown in Table 2 with MI= 0.73 and the switching timing angles q_i as: (9.54, 20. 07, 26.70, 39.37, 52.34, 58.38, 67.49°) the output voltage will be equal to the ac system voltage, i.e. V_1=13.8kV, and the reactive power exchange between 15-level VSI and the ac system will be zero. By varying the amplitude of the three-phase output voltage produced by 15 level VSI using different values of MI above and below 0.73, the inverter generates or absorbs reactive power from the ac system ($\times Q_c$). The system shown in Figure 7 is simulated using the PSCAD/EMTDC, simulation program. The results of the simulation are shown in Figures 8 and 9. In Figure 8 the output line voltages of the 15-level VSI, U_{12}, U_{23}, U_{31}, the spectrum of harmonics present in U_{12}, Q_c reactive power produced by that, together with line system voltage U_{ab}, 3 binary dc input voltages and also rms value of the inverter output voltage V_{rms} are illustrated. It is seen that the output voltage is almost distortion-free. The produced reactive power of the inverter was stepped at t_1= 0.4, t_2= 0.7 and t_3= 1s using different triggering control angles, q_i from Table 2 when MI is respectively 0.68, 0.8 and 0.73. The resulting step responses for the generated reactive power Q_c and instantaneous

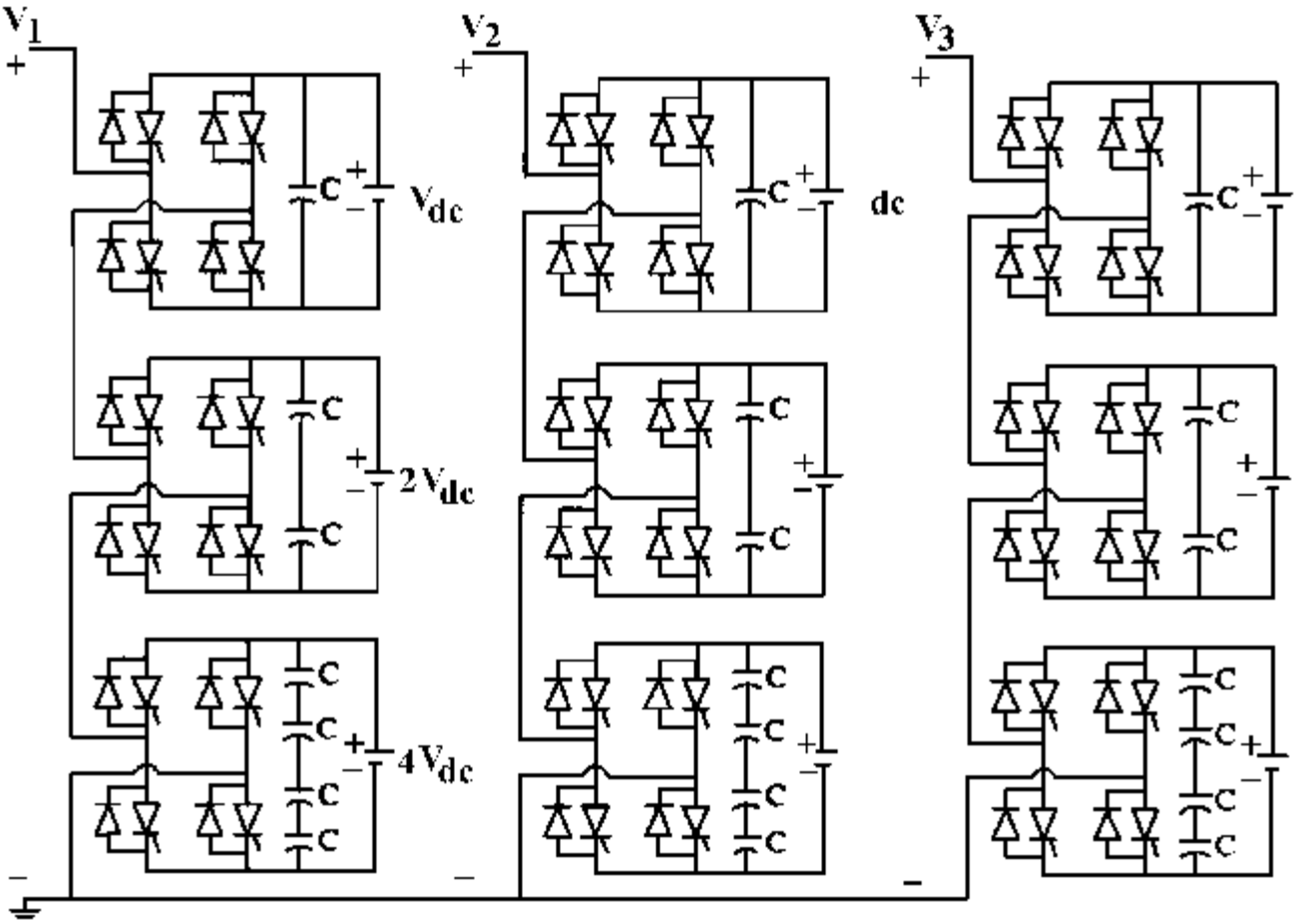

Figure 6. Three-phase star connection of (BMVSI).

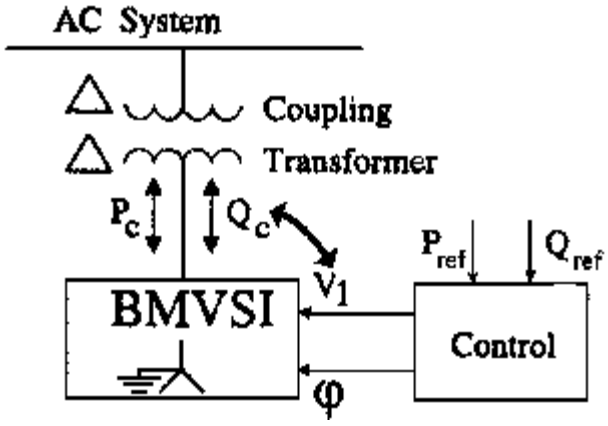

Figure 7. A Three-phase 15 level VSI connected to A 13.8kV power system.

values of the output voltages of the inverter which create the dynamic capability of this compensator, are shown in this figure, e.g. at t_2 = 0.7s, this 15-level VSI is capable of making almost 9 MVAR change in less than 0.1 second.

Similarly, the real power exchange between the inverter and the ac system can be controlled by phase shifting the inverter output voltage with respect to the system voltage, i.e., the inverter supplies real power to the ac system, if the inverter voltage output is made to lead the corresponding ac system voltage. By the same token, the inverter absorbs real power from the ac system, if the inverter output voltage is made to lag the ac system voltage. Figure 9 shows the ability of the 15-level VSI to make a 50 MW transition in a few cycles by leading or lagging the output line voltage U_{12} by 30° with respect to the system voltage U_{ab}. The inverter three-phase currents when the output active power of the inverter is 26 MW are also illustrated in this figure.

The transient simulation results for a

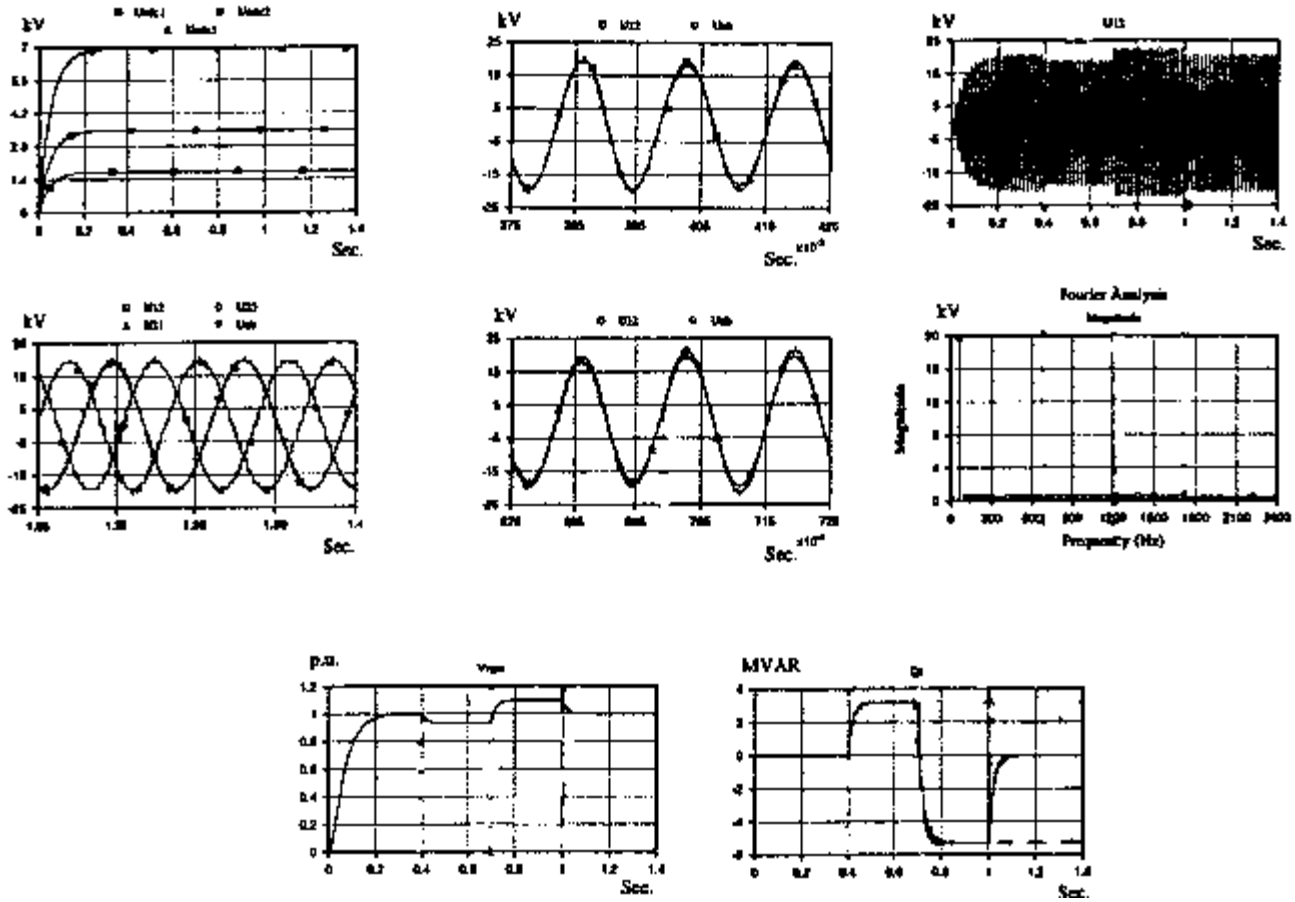

Figure 8. Simulation results showing the capability of 15 level VSI to establish positive and negative reactive power flow.

single-phase to ground fault at load bus are shown in Figure 10. The fault path has zero impedance. The load is 8 MW+ j10 MVAR. The SVG is supplying 11 MVAR leading vars. Initially the capacitor voltages are maintained at 2, 4 and 8 kV levels modulating the conduction period of each capacitor to control their voltages in a binary proportion. The results confirm the ability of SVG to dynamically compensate the system and restore the system to its prefault state once the fault is cleared after eight cycles fault at 0.35s.

Figure 11 shows the star connection of the three-phase structure of the proposed SVG in Figure 3. This configuration is used for the test system to illustrate three-phase simulation results.

The operational performance of the three phase 13 level inverter based SVG shown in Figure 11 was evaluated using PSCAD/EMTDC simulation program. A model distribution system is shown in Figure 12 which includes the above mentioned SVG directly coupled to a station bus. A remote varying load is connected through a distribution feeder.

The distribution system considerd is 13.8kV, 60Hz with short circuit capacity of 100MVA. With normalized per unit modulation index MI= 0.7 the switching timing angles q_i are (14.265, 24.070, 37.800, 53.576, 57.866 and 66.297°) and dc side voltages rated at 4.214kV and 8.428kV in each phases, the output line voltage will be equal to the ac system voltage, i.e. 13.8kV. Therfore the reactive power exchange between 13-level SVG and the distribution system will be zero and also by

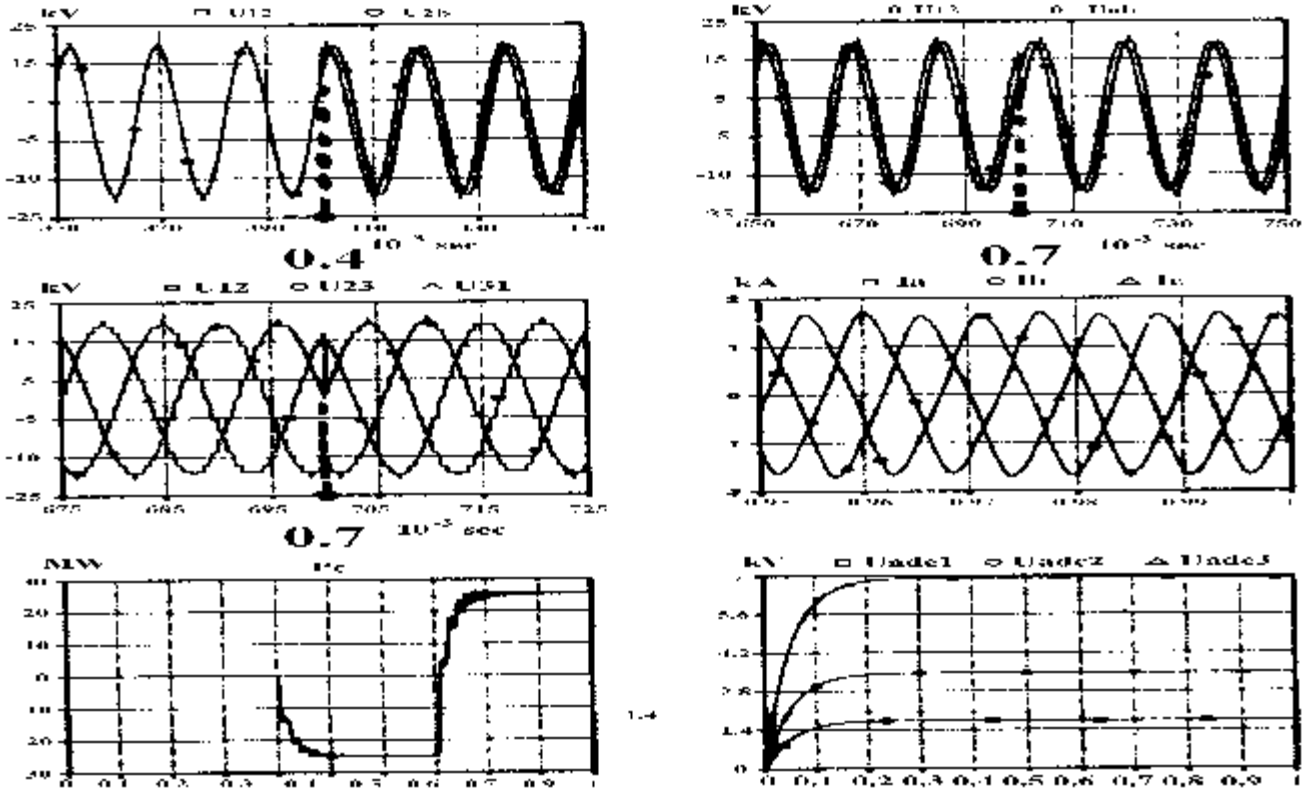

Figure 9. Simulation results showing the ability of 15 level VSI to create positive and negative power flow.

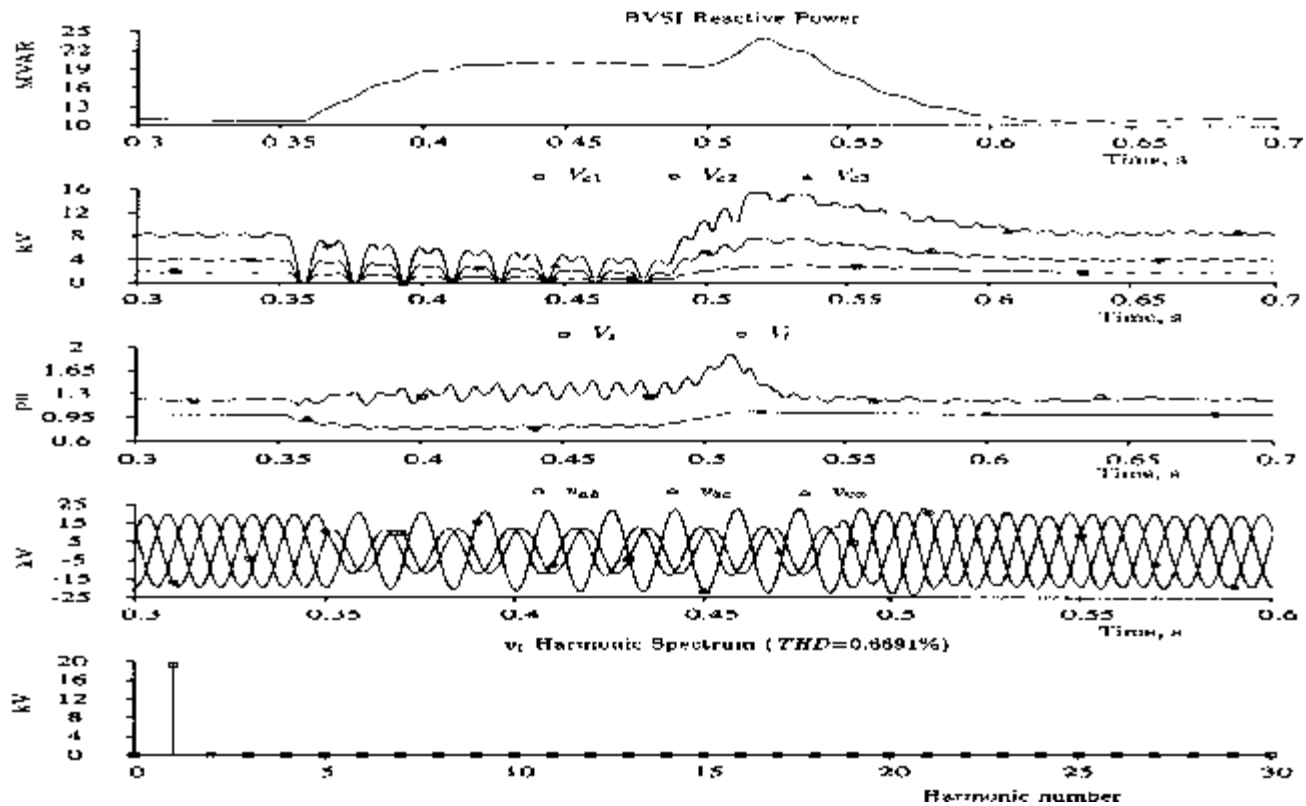

Figure 10. Single phase to ground fault at load bus using 15 level SVG.

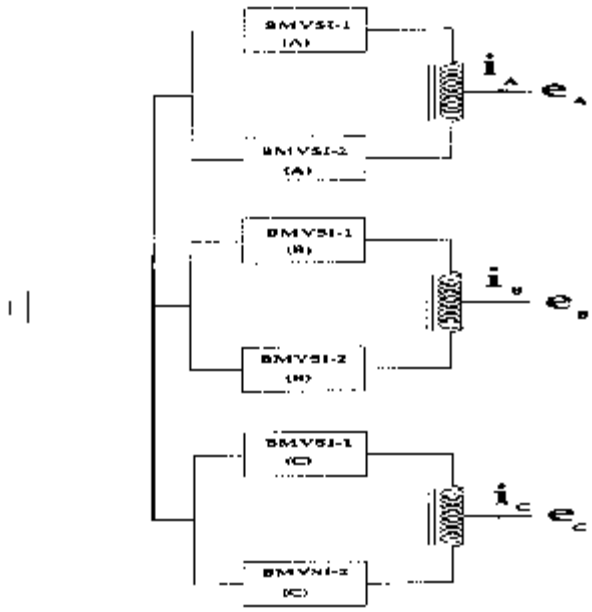

Figure 11. Three-phase star connection of proposed transformer-less binary multilevel converter (SVG).

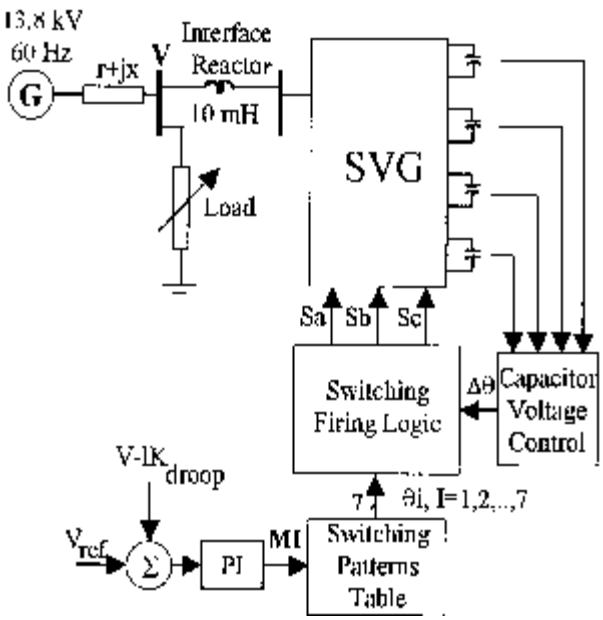

Figure 12. Three-phase 13 level SVG connected to a 13.8 kV power system.

varying the amplitude of the three-phase output voltage produced by 13-level SVG using different values of MI above and below 0.7, the SVG is capable to generate or absorb reactive

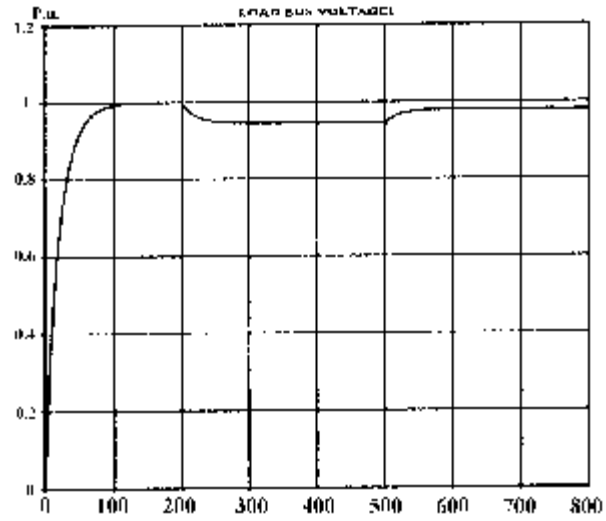

Figure 13. Bus voltage variation with step changes in the load demand without connection of compensator.

power from ac system. In Figure 12 a special algorithm which provides active control over each capacitor voltages is used. The capacitor voltages are compared to their corresponding referance voltage and an error signal which is filtered and used to phase shift a specific portion of the SVG output voltage. The direction of the phase shift depends upon whether the SVG is producting leading or lagging vars. The capacitor controller is disabled when the SVG's current output is very low in magnitude. To regulate the load bus voltage, proportional plus integral (PI) controller with feedback signal derived from the voltage at load bus (V) and the reactive current (I) flowing into the SVG weighted with V-I characteristic droop i.e. K_{droop} =1% is employed. The output of the PI controller is the modulation index (MI) and depending upon its value, the switching timing angles q_1, q_2, q_3, q_4, q_5 and q_6, to turn on and off various switches are selected from the precomputed switching patterns table. The capacitor voltage controller generates Dq_i.

These angles and the gate firing angles are processed through swith firing logic algorithm to modulate the conduction period of each capacitor to control their voltages in a binary proportion. The switch firing logic generates the

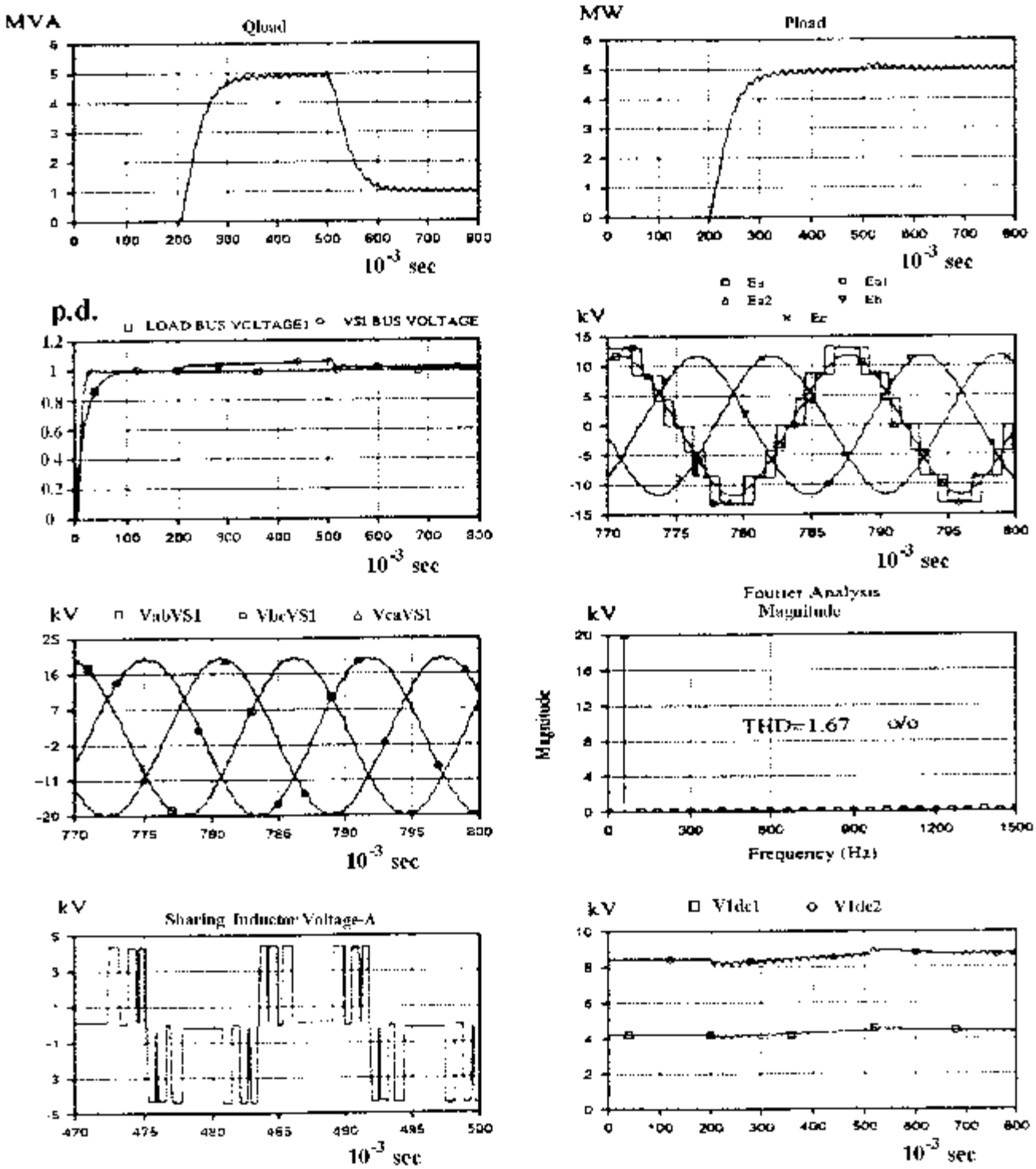

Figure 14. Simulation results showing the dynamic capabiliitly of 13 level SVG in power system environment.

appropriate gate firing pulses S_a, S_b and S_c.

PSCAD/EMTDC simulation results of the proposed system are shown in Figures 13 and 14. As it is seen in Figure 13 at 0.2 second and 0.5 second, a step changes in three phase load i.e. 5+ j5 MVA and j4MVAR is applied, the

system voltage drops corresponding to the values of the load changes without the SVG. But when SVG is used, for the same step changes, the output system voltage drops and restored rapidly as seen in Figure 14. The phase voltages of SVG along with the spectrom of harmonics present in line voltage of SVG are also shown in this figure. It is seen that the outpot voltage of this SVG is almost distortion free. The voltages on each side of the dc bus capacitor and also the voltage across the current sharing inductor L for phase A is also illustrated in this figure. These simulation results show the effectiveness of the proposed SVG configuration and also the switching strategy, in other words it is a good tool for dynamic compensation of a distribution system and it can be used for dynamic stability improvement of the power systems.

CONCLUSIONS

In this paper, a new SVG using parallel connections of BMVSI by means of current sharing reactors is introduced. For larger capacity of power system compensation paralleling the BMVSI would be promising for high voltage high power applications. Using appropriate switching strategy, the lower order harmonics in the output of the proposed SVG are eliminated, therefore dynamical compensation of a distribution system becomes possible without creating aditional harmonic pollution for power systems environment.

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