TRANSIENT MINIMIZATION WITHIN STATIC VAR COMPENSATED DISTRIBUTION SYSTEMS

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Abstract VAR support should be supplied as close to the load as possible to minimize transmission losses. For voltage control and for improvement of total power factor in a distribution system the circuit-breaker switched capacitor banks can be used. The problems with this solution are the voltage steps caused by the large sizes of the capacitor banks as well as the transients caused on insertion. Thyristor-switched capacitors (TSC) as applied to distribution systems are the main focus of this paper. The advantage of thyristor switching is that finer and frequent switching can be used without wear on the switching element. In addition, the thyristor can give "point on wave" switching with the potential of very low transients on insertion or removal. The interaction of inrush-limiting inductors, the supply transformer and also the effect of initial conditions of capacitor banks to minimize transients have been studied. In this paper transient minimization is examined by simulation and confirmed by experimental studies.

Key Words Static VAR Compensators, Thyristor Switched Capacitors, Transient Minimization

چکیده یکی از روشهای کنترل ضریب قدرت و افت ولتاژ در شبکه های توزیع انرژی الکتریکی استفاده از خازنهای کنترل شده تریستوری می باشد. دراین مقاله کمینه کردن جریانهای گذرا موقع وصل خازنها به شبکه مطالعه شده است. کمینه نمودن جریانهای گذرا بکمک عمل پرکردن خازنها توسط یکی از تریستورهای موازی معکوس قبل از موازی کردن آنها به شبکه امکان پذیر می گردد. اثر راکتور اضافه شده به خازن وراکتانس ترانسفورماتور درکاهش گذرا وانتخاب زمان مناسب وصل خازن وقتی خازن از قبل پرشده باشد مطالعه شده و نتایج بدست آمده از مشابه سازی مدار و همچنین نتایج عملی و آزمایشگاهی دریک شبکه توزیع انرژی الکتریکی ارائه شده و نشان داده شده که عمل پرکردن خازنها و انتخاب زمان مناسب وصل آنها به شبکه درکاهش و حذف جریانهای گذرا مؤثر می باشد.

INTRODUCTION

Static VAR compensators (SVC) are usually used to control the supply of VARs to power systems by switching reactors or capacitors in shunt with the transmission or distribution system. They enable the voltage or VARs of the bus at the location of the SVC to be controlled. The response time of an SVC is in the range of a few cycles and when thyristors are used they can be switched as often as the control requires. Switched banks can be regulated automatically to control variations in bus voltage [1]. Hence, an SVC provides a fast response to the VAR needs of a transmission or distribution system. Rapidly varying loads cause voltage fluctuations in the transmission or distribution system. Arc furnaces, electric traction loads, large pumps and compressors, mining hoists and car crushers are examples of rapidly varying loads. SVCs are fast enough to stabilize voltage for these applications, that is reduction or elimination of flicker, low voltage, etc. The SVC supplies the transient VAR requirements to return the system voltage to its nominal level. SVCs can also be used to balance unbalanced loads as seen from the transmission or distribution system [2,3]. Examples of unbalanced loads are arc furnances and electric traction loads. Several

types of SVC are in use:

- Thyristor-switched capacitor (TSC);
- Thyristor-switched reactor (TSR);
- Thyristor-controlled reactor (TCR).

The purpose of this paper is to study the use of three phase subdivided capacitor banks at a given distribution system, with separate thyristor control of each bank. A TSC is a shunt capacitor bank with back-to-back thyristors which should be switched on when the voltage across the thyristor switch is zero, and the thyristor switches itself off at current zero. The capacitor is avaliable for switching every cycle. When a capacitor bank is switched, it is known that the steady state bus voltage changes by an amount proportional to the size of the capacitor that is switched. In this paper a study is made to show the interaction between inrush limiting inductors, supply transformer impedance and initial conditions on the capacitors. Studies in which the performance of the system is simulated, enable the choice of parameter values and a control scheme which minimizes transients at switching. The correct firing of the thyrisors provides low transients on first insertion and ideally no transient on any subsequent changes between banks.

SYSTEM MODELLING AND CAPACITOR SWITCHING

Switching of capacitors is more difficult than switching an inductive load current. When a thyristor breaks current it does so at about current zero, which for a capacitor is when the system voltage wave is at its maximum; for first energising of a capacitor bank, the "inrush current" can be several times the rated current of the bank and the transient current continues for a few cycles. To reduce the transient effects at first insertion of a capacitor bank, an inrush current-limiting reactor is connected in series with each phase of a bank. This inrush reactor also limits the "outrush current" which occurs when there is a short circuit on the system, and all the capacitors discharge into the fault. Another way to reduce transients is to turn on at a preferred time e.g., when the voltage across the switch is zero.

Figure 1 shows the simplified one-line diagram for a switched capacitor bank with series inrush current-limiting reactor. A TSC consists in general of n capacitor banks, each in series with a solid-state switch. The number of banks n is determined from practical considerations that include the operating voltage level, maximum compensation requirement, current rating of the solid-state switches, etc. The solid-state switch in series with the reactor bank is composed of a reverse-parallel connected thyristor pair. The solid-state switch offers more operating flexibility than a circuit breaker in connection and disconnection of the capacitor banks from the ac system, because the time within the cycle when connection takes place can be controlled.

Let it be assumed that $v = V_m Sin(\omega t)$; if the first firing angle of thyristor T_1 is chosen when the voltage across the switch is zero and then at the peak voltage e.g., $\omega t = 0$, $\frac{3\pi}{2}, \frac{3\pi}{2} + 2\pi$, ...and the firing angle of thyristor T_2 at $\omega t = \frac{\pi}{2}, \frac{\pi}{2} + 2\pi, \frac{\pi}{2} + 4\pi$, ...the voltage across the capacitor bank C_1 will be:

$$V_{c1}(t) = \frac{\omega\omega_0}{\omega^2 - \omega_0^2} V_m \left[Sin(\omega_0 t) - \frac{\omega_0}{\omega} Sin(\omega t)\right] \quad (1)$$

and the current of capacitor will be:

$$I_{c1}(t) \frac{C_1 \omega \omega_0^2}{\omega^2 - \omega_0^2} V_m \left[Cos(\omega_0 t) - Cos(\omega t)\right] \quad (2)$$

where $\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$ is the resonant frequency of the L_1, C_1, V_m is the peak voltage and ω is the source frequency. In practice the first part of Equation 1 or $\frac{\omega \omega_0}{\omega^2 - \omega_0^2} V_m Sin(\omega_0 t)$ occurs only for a few periods because of the damping resistance of the power system not modelled here. This first insertion of a capacitor bank produces high harmonic current in the capacitor superimposed on the normal 50Hz current. Also the voltage across the capacitor is higher due to the combination of the normal 50Hz voltage and the voltage due to the harmonic current. The transient current is

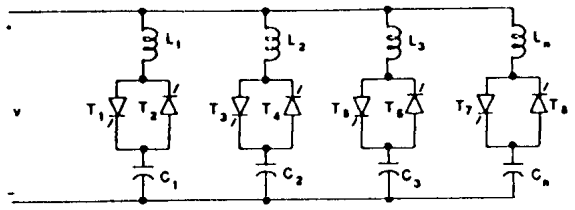

Figure 1. Single line diagram for a thyristor switched capacitor.

at a frequency f_0, the resonant frequency between L_l and C_l.

For correct simulation appropriate models for all components need to be selected. The distribution system can be modelled as a three-phase balanced sinusoidal source. To this is connected the resistance and the inductive reactance of the distribution system in series. This series impedance Z_n can be calculated by: $Z_n = \frac{U_n^2}{S_{s.c.}}$, where U_n is the nominal line voltage of busbar of distribution system and $S_{s.c.}$ is the short circuit level of the distribution system at 11kV busbar. Figure 2, a simple model of a transformer, can be used without significant loss of accuracy and without parallel magnetic circuit. The load must be modelled by an equivalent circuit of a shunt resistance in series (or in parallel) with a shunt reactance according to the specified real and reactive power or power factor. With high variation of loads the voltage of busbar varies, the voltage

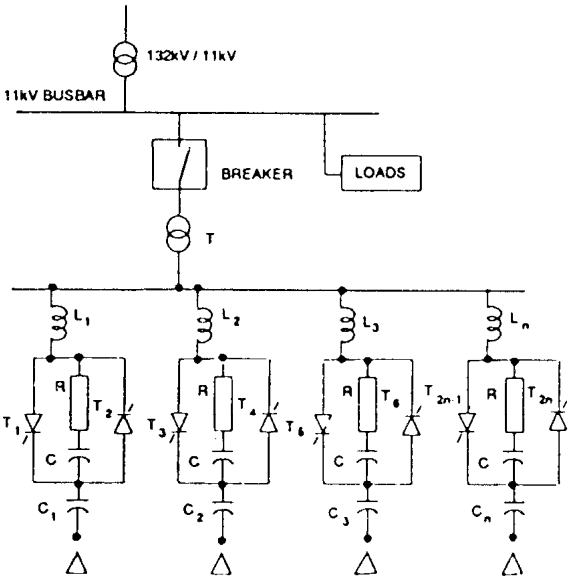

Figure 2. One-line representation of a TSC type compensator

drop on the busbar can be expressed [4] as a function of the active and reactive power flows through it, and as the load varies it will also vary with time; hence:

$$\Delta V(t) = \frac{R}{V_n} P(t) + \frac{X}{V_n} Q_L(t) - \frac{X}{V_n} Q_c(t) \qquad (3)$$

The voltage support by the TSC is described by (3), where R and X are the series resistance and reactance of the whole distribution system respectively, P and Q_L are the real and reactive powers flowing through the busbar and Q_c is the reactive power produced by TSC and $V_n = \frac{U_n}{\sqrt{3}}$ is the nominal phase voltage of busbar.

The functional block diagram of a thyristor switch capacitor (TSC) type compensator is shown in Figure 3; where the back-to-back thyristor pairs are in parallel with a snubber circuit (R-C) chosen to reduce the $\frac{dv}{dt}$ across the thyristors. Typically the values of the protection components will be C, 0.01 to 2 μF; R, 10 to 2000Ω; and L, 50 to 200μH [5].

By the following control scheme a quantized proportional control scheme can be introduced:

$$N_{bank} = \begin{cases} N + m & if \ \frac{\Delta V}{\Delta V_{max}} \geq m \\ N & if \ \frac{\Delta V}{\Delta V_{max}} < 1 \\ N - m & if \ \frac{\Delta V}{\Delta V_{max}} \leq -m \cdot h \end{cases} \qquad (4)$$

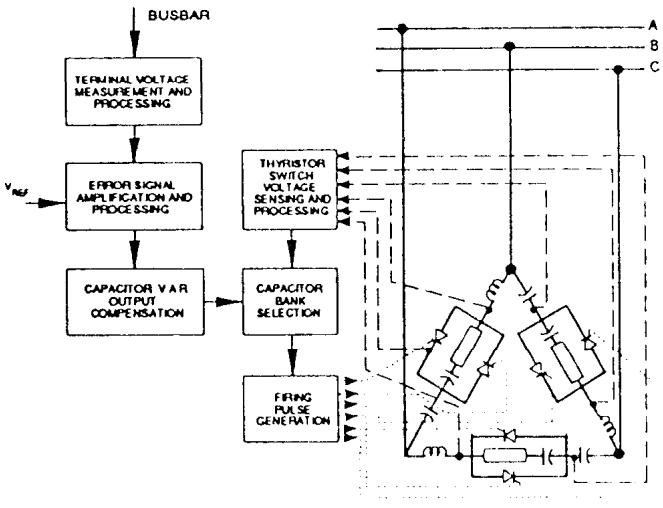

Figure 3. Functional block diagram of a TSC type three-phase delta connected compensator

where:

- N_{bank} is the bank number which is required to put into the distribution system
- N is the bank number which has been put into the system before the auto control has been chosen
- m is the number which is smaller than 8-N
- h is the hysteresis introduced

In order to avoid the instability of compensation or the oscillation at the bank(s) change-over point, hysterisis must be introduced into the control algorithm, as seen in Figure 4.

The only specification of the control scheme which is entered by the operator according to the controlled system is the maximum voltage variation. And the hysteresis introduced is also determined by it.

The auto control mode should be entered in the condition when the voltage is manually set to the reference voltage where the compensated VARs is at the middle point of its compensation capability. That will ensure the TSCs has the maximum positive and negative swing capability before the compensation thresholds are met.

There are several ways which may be introduced for the accurate timing of the control, especially the DPLL (digital phase lock loop) which is the one most often used in the microprocessor-based control system. But there are

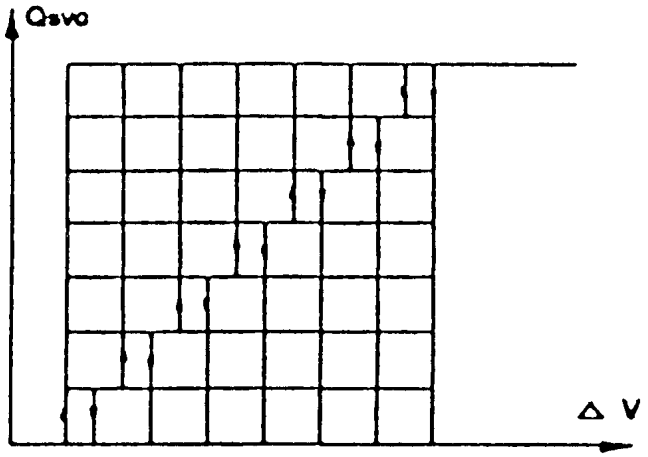

Figure 4. Voltage control character of a TSC bank

three independent DPLL modules which should be introduced for each of the three phases in most of the applications.

With the MCS-96 microcontroller, the synchronization of three phase may be simplified by using the HSI (High Speed Input) and its software timers.

The present implementation is synchronizing the AB phase and the other phases are time shifted with respect to this.

SIMULATION AND REDUCTION OF TRANSIENT IN A T.S.C.

Here we study the effect of the supply transformer impedance, auxiliary components and initial conditions on switching transients of the TSC.

Influence of Supply Transformer and Auxiliary Components

The circuit of Figure 2 with two delta-connected banks of capacitors has been simulated on special purpose power electronic software (ATOSEC5) [6] and the performance with different transformer impedances is studied. For the simulation the phase voltage amplitude of the source is $V_m = 240\sqrt{2}$ volts and its frequency is $f = 50$Hz. The capacitance of first delta connected bank is $C_1 = 33.5\mu$F in each branch. The capacitance of second delta connected bank is $C_2 = 67\mu$F in each branch. The inrush-limiting inductor of each capacitor in first bank $L_1 = 50\mu$H and in second bank $L_2 = 100\mu$H.

Figure 5 illustrates the transient voltages across the capacitor banks when the initial switching occurs at the zero crossing of the mains voltage. Subsequent switching occurs at mains voltage peaks. The voltages across the capacitor banks and the transient currents through the capacitor banks (X1 and CX1 for first phase of first bank, X4 and CX4 for first phase of second bank and X22 current through one line of the transformer T) are illustrated when the capacitor banks are initially uncharged. It can be seen

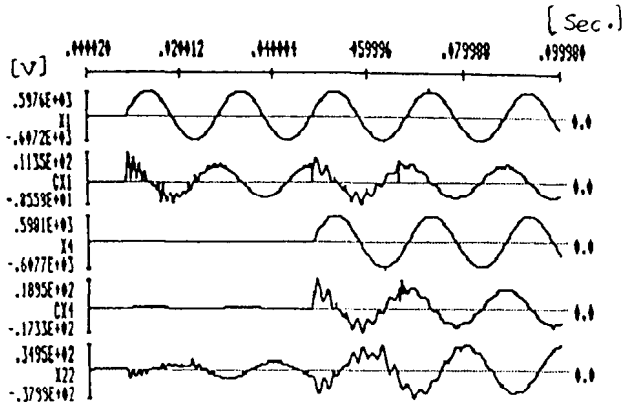

Figure 5. Transient voltage and current of three-phase capacitor bank with low power rating of transformer

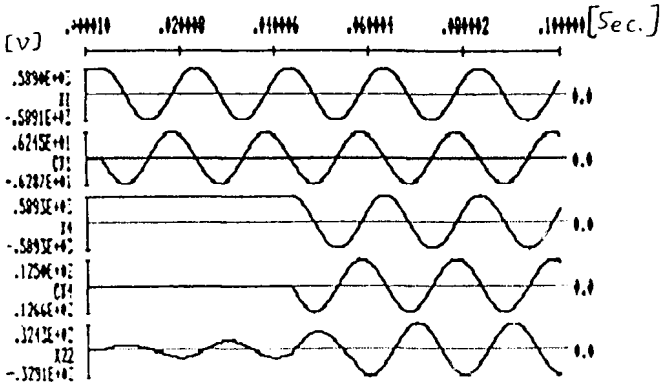

Figure 6. Simulation results for three-phase precharged capacitor switching

that the waveform of the transient voltage includes many spikes due to the first energising of capacitor banks with a high value of the transformer inductance (L_T= 500 μH).

When the circuit is simulated with a lower inductance (L_T= 100μH), the results show a proportional reduction in the peak of the transient terms as well as an increase in transient resonant frequency. So, to minimize the transients, a transformer with a high level of short-circuit power is preferred, but because of the zero initial conditions on the capacitors at first switching time, the transient cannot be reduced to zero. When a single capacitor bank is used, the influence of inrush-limiting reactor is similar to that of the transformer reactance. However, when more than one bank is to be used, limiting reactors must be used to limit the flow of current from the first set of capacitors. When the second bank is switched on, the simulation results show these limiting reactors reduce the transient at the moment of insertion. However, transients still occur and can give rise to objectionable disturbances. Whilst simulation studies showed that variation in component values influenced the transient, an alternative was sought in an attempt to reduce them significantly.

Influence of Initial Conditions on the Capacitor Banks

If all of the capacitor banks are precharged to the peak value of the source voltage, and switching occurs when supply is at its peak (i.e. no volts across the switch), transients reduce considerably. The case shown in Figure 2 with precharged capacitor banks is analyzed next and as Figure 6 shows transient current and transient voltage decrease significantly, so the correct firing of the thyristors with precharged capacitors provides low transients on first insertion and ideally no transient on any subsequent changes between banks. In Figure 6 the instantaneous change from one bank energized to the other bank being used shows the smooth transition that could not be achieved by mechanical switches. The switching occurs at the instant of matching of the initial conditions for capacitor voltage and inductor current. Ideally when both conditions are matched there will be zero transients on switching. The components of the source impedance will alter this exact matching as the presence of the capacitor will change the mains voltage at the capacitor bus and hence the boundary conditions of the source. For most cases this supply impedance has a very small influence on the boundary conditions and a low transient results. The precharging thus significantly reduces the transients over the case of switching an uncharged capacitor. The added benefits are a reduction in the $\frac{dv}{dt}$, $\frac{di}{dt}$ and peak reverse voltage stresses on the switches. The question arises of how to precharge the capacitors without additional components.

Soft Precharging to Minimize Transients of a T.S.C.(Simulation)

Let us consider the cases of switching a partly charged

or an over charged capacitor at various points of the mains cycle (Figure 7). From the waveforms we can find the optimum switch-in angles which lead the minimum transient into the power system. They are:

$$\alpha = \begin{cases} \frac{3\pi}{2} & \text{for} \quad \frac{U_{c0}}{U_p} \leq -1 \\ \pi - Arcsin\left(\frac{U_{c0}}{U}\right) & \text{for} \quad -1 < \frac{U_{c0}}{U_p} < 1 \\ \frac{\pi}{2} & \text{for} \quad \frac{U_{c0}}{U_p} \geq 1 \end{cases} \qquad (5)$$

where:

- U_{c0} = Voltage to which the capacitor is charged
- U_p = system peak voltage

This equation shows that for low transient insertion, the switching shall take place, when the magnitude of voltage across the thyristor is at its minimum value.

When the thyristor is turned on at the peak of the voltage wave, and the capacitor is fully charged, the inrush current may reduced even to zero. So the optimum position of switch-in is the point when the system voltage is at its peak while the capacitor is fully charged. The capacitor are left fully charged when turned off and thus if they are always turned off at the positive voltage peak, they will be in the best condition for low transient bank change over.

The question arises of how to charge the capacitors initially. One option is to use an auxiliary-charging circuit, but this is not necessary. Using the main thyristors, the capacitor charge can be increased in small increments at each mains cycle with low current pulses.

The way in which the capacitors are precharged in the system is to charge the capacitor gradually in small steps with the aid of a microcontroller. That is, firing on the positive thyristors of each bank at $\omega t = \pi$-a, 3π-2a, 5π-3a, ..., where a is the angle sufficiently small so that the charging pulse current is kept within acceptable limits.

The case of a= $\frac{\pi}{50}$ was simulated and the results are shown in Figure 8. Here X2 shows the capacitor voltage charging to the peak of the mains voltage over one second. The curve X1 shows the voltage across the snubber capacitor and X7 is the current through the thyristor charging the capacitor.

EXPERIMENTAL RESULTS

A single phase circuit for switching two banks of capacitors (33.5μF and 67μF) was constructed and thyristor firing was coordinated by a microcontroller. The thyristor switches were constructed with two series devices to handle the peak reverse voltage of 1176 Volts associated with 415 V operation (see X1 of Figure 8). .

The firing of thyristors occurs at a particular angle with respect to the mains voltage. In the microcontroller the

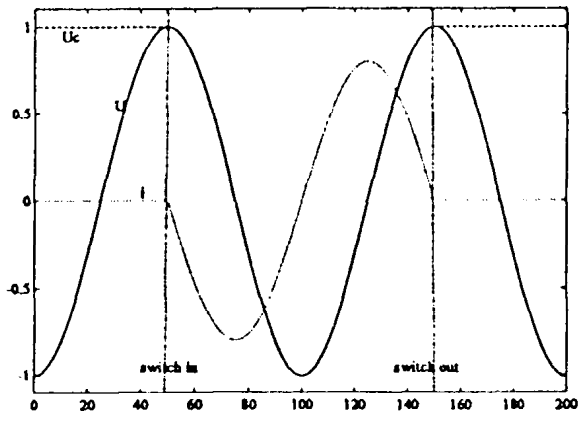

Figure 7. Firing of minimum transients

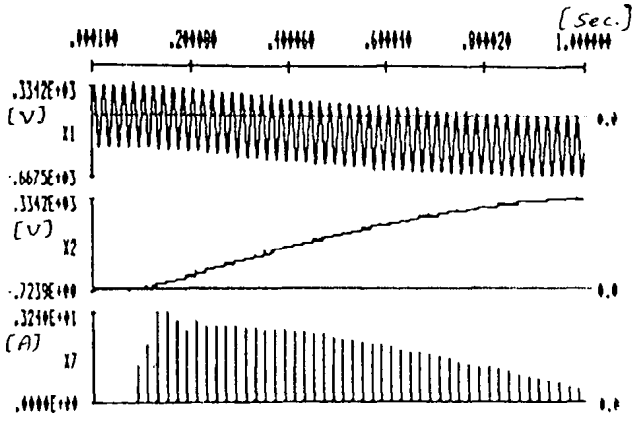

Figure 8. Simulation of gradual precharging of capacitor banks

zero crossing of mains is used as the reference for all firing instants. For precharging of the capacitor banks the firing is commenced at angle 0 before the negative zero crossing. In the Intel 80C196 microcontroller the firing time of the High Speed Output (HSO) lines is written to a device register. When the clock matches this time the line goes high without intervention from the processor. The processor increments the firing angle at each cycle; when firing is occuring at the peak of the voltage wave the capacitor bank is considered as charged and is available for switching. When all banks are charged the signal to change between banks can be modified once per cycle. At the peak of the mains, voltage wave the negative conducting thyristors of the selected banks are fired. Any bank not fired remains in the positive charged state and change over between banks gives a smooth change of current on its zero crossing.

In Figure 9 the charging of the capacitors of one bank is shown. The firing angle was incremented in 1500 steps, once per cycle giving a soft charging over a period of 30 seconds. At this charging rate the current is negligible compared to the operating current. Figure 11 shows the firing of a charged bank. Little transient is seen in the voltage or current waveforms. The changing between one capacitor bank and another can occur with negligible transient current as shown in Figure 12. Figure 10 shows the charge-maintainance.

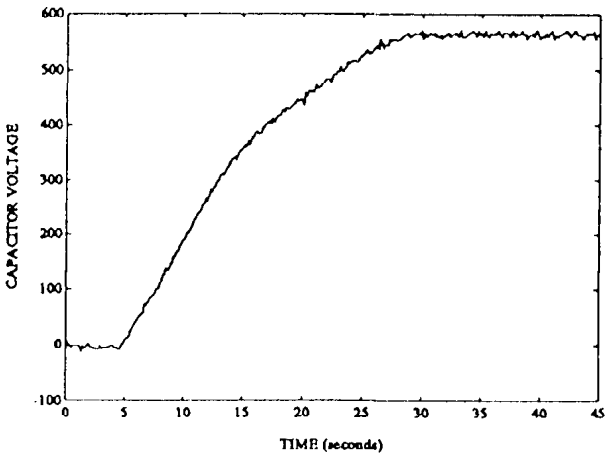

Figure 9. Voltage of capacitor banks during precharging

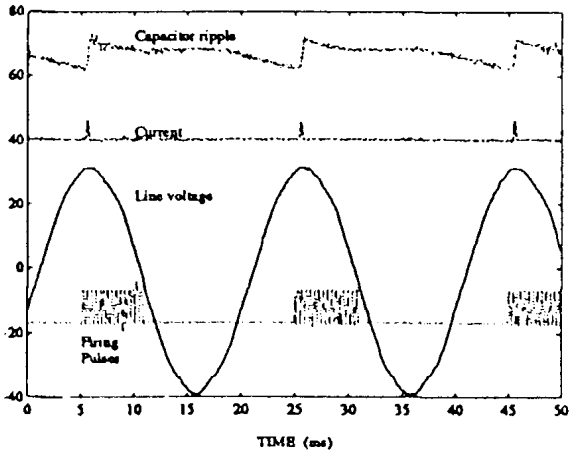

Figure 10. Charge maintenance of capacitor banks

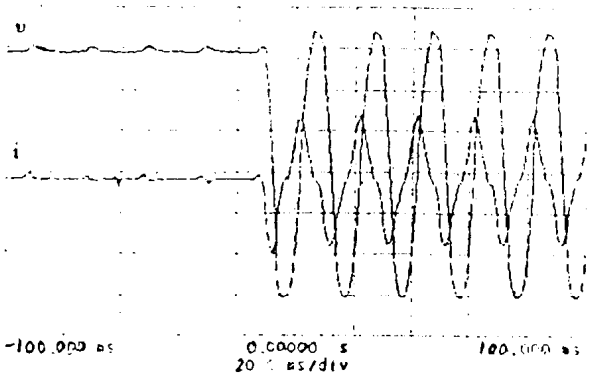

Figure 11. Experimental results for precharged capacitor-bank switching

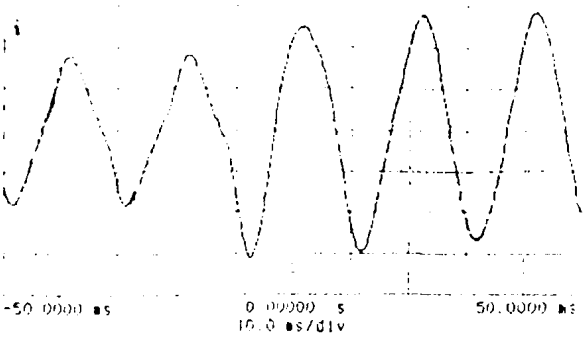

Figure 12. Changing between banks-experimental current results

With the aid of the MCS-96 microcontroller, a test on a 40KVA 415KV experimented TSC confirmed the transient reduction properties of the computer simulation.

Due to the increasing need of the good quality power supply transmission, the approach taken in this paper should be a useful model for the cost-effective application of TSC to distribution systems.

CONCLUSION

The transients in a thyristor-switched capacitor need to be controlled by series inductors in case of any misfiring of thyristors. The main benefit of the use of thyristor switching is that with precharging, the transients can be effectively zero.

A microcontroller-based scheme to control the firing of the thyristors for the precharging of the capacitors and the changeover between banks has been developed. The experimental results confirm the simulated results of low transient operation.

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