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Hierarchical Control Strategy of Constant Power Load-based DC Micrograds using a New Distributed Averaging Proportional Integral Secondary Controller

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Dedicating more attention to renewable energies and power electronic improvements results in increased direct current microgrids (DC MGs) application. However, DC MGs have some challenges with voltage adjustment and power sharing. To do so, a two-layer hierarchical control structure, including a new fully distributed secondary control strategy and conventional primary droop control method, is proposed and employed in this paper to share power and swiftly adjust the voltage accurately. Indeed, a distributed-averaging proportional-integral (DAPI) secondary control strategy is introduced. Another problem in DC MGs is the existence of constant power loads (CPLs), which may result in instability. To overcome the problems caused by CPLs, a term based on the output voltage of CPL is added to the proposed DAPI to prevent instability. The required control inputs are obtained using localized data of the DC bus and their neighbor's secondary control inputs inspired by cooperative control. Besides, this strategy needs no knowledge of the microgrid topology, which enhances flexibility. For validating the proposed DAPI strategy in DC MGs, an islanded DC MG is simulated in the MATLAB/SIMULINK software. Comparing the results with those obtained from another existing method proves the performance of the proposed DAPI controller under different scenarios of plug-and-play, communication failure, and load changes.

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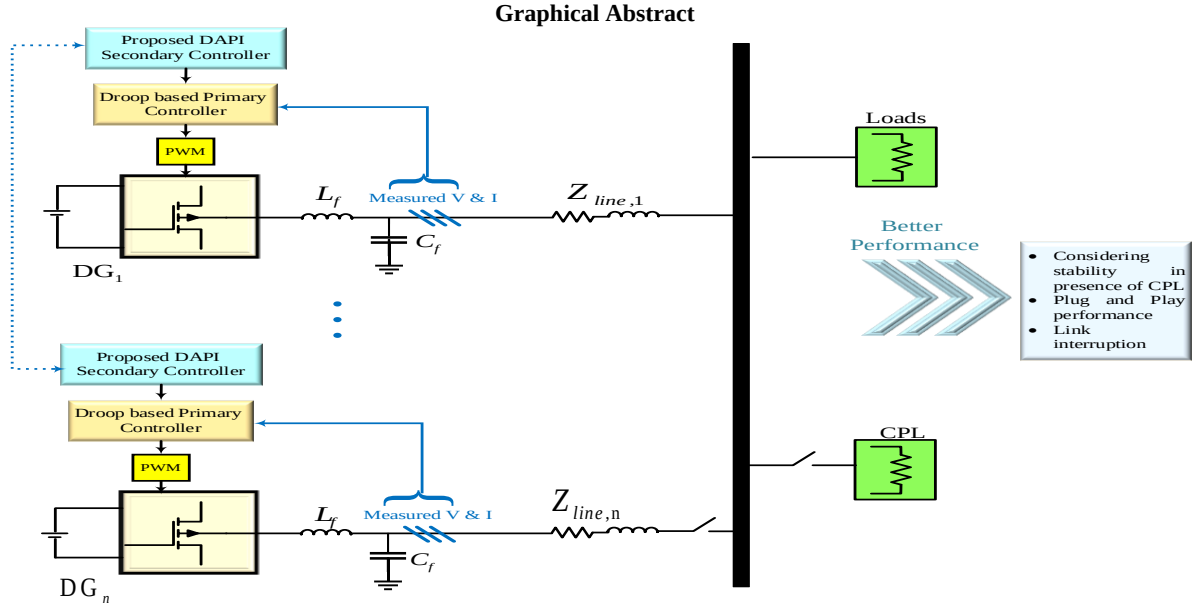
Graphical Abstract



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1. INTRODUCTION

Since 19th century, AC grids have garnered attention among researchers due to their capability to transform several voltage levels and cover wide areas by transmitting power to removed areas (1). Despite their benefits, the high costs and challenges associated with expanding and constructing new power plants and transmission lines to meet the growing demand and advancements in power electronics have prompted the adoption of DG grids. The utilization of microgrids (MGs) has surged due to the integration of DC-based renewable energy resources (2, 3). The reduced power and voltage conversions required, along with fewer losses and the absence of reactive power and frequency-related issues, have further promoted the adoption of DC MGs.

In a DC MG, several distributed generations (DG) units such as storages, loads, and controllers exist. The controllers are responsible for regulating the voltage and accurately distributing power among DGs (4). Various strategies have been studied and employed to control DC MGs, which can be categorized as centralized and decentralized schemes (5). Among all, hierarchical control strategies have received attention due to their high reliability and flexibility. This method consistently implements the primary level by the droop strategy surveyed in literature (2, 6, 7) for DC MGs. Even though the droop controller works appropriately, it has some drawbacks. A trade-off between voltage regulation and current sharing should be considered (8). The secondary level is utilized to address limitations (9, 10). In most research, distributed manner-based controllers outperform other schemes because a sparse communication graph can be utilized without the need for central controllers, resulting in high reliability (11).

Previous studies have utilized various types of distributed methods (12-21). A comprehensive and descriptive multilevel distributed hybrid control architecture has been implemented by Mathew et al. (12) for an isolated low-voltage DC MG to address the limitations of centralized and decentralized control strategies. A cooperative distributed method has been implemented by Nabian Dehaghani et al. (14) and Biglarahmadi et al. (13) to control the DC subgrid of a hybrid AC/DC MG. Nabian Dehaghani et al. (15) proposed a cooperative distributed voltage and current control-based secondary level for DC MG in the presence of noise. In this setup, two DGs are connected through boost converters, while the other two are connected through buck converters. Li et al. (16) presented a distributed cooperative control approach for islanded DC microgrids. The approach utilizes a dynamic consensus algorithm to estimate the average voltage for each agent. Additionally, a unified voltage closed-loop controller is employed to achieve voltage adjustment and load-sharing control objectives. Another distributed control strategy is discussed by Morstyn et al. (17) for a DC MG in seamless mode transitions between various operational modes, including islanded and grid-connected operations. A distributed secondary control scheme is presented by Guo et al. (18) for islanded DC MGs to allocate power and restore voltage. Their proposed strategy involves a feedback loop, in contrast to the feed-forward approach used by other existing literature. A consensus-based distributed finite-time secondary controller is introduced by Sahoo, and Mishra (19) to achieve its objectives within a finite settling time in DC MGs. For sharing the power of loads proportional to DGs' power ratings and restoring the voltage by load changing, a power rating-based shifted voltage technique is recommended by Dam and Lee (20). The proposed distributed strategy results in less voltage drop, ensuring that voltages remain constant regardless of load variations. Xing et al. (21) introduced a dynamic average consensus-based distributed secondary control scheme to achieve voltage adjustment and current sharing within a fixed settling time. However, a few research studies have focused on the consistent presence of power loads (CPLs).

Most of the aforementioned works employ traditional straightforward control approaches. However, this paper aims to propose a scheme called the Fully Distributed-Averaging Proportional-Integral (DAPI) controller to achieve its goals. This protocol is thoroughly investigated in AC MGs. For instance, a distributed averaging PI controller is adopted by Schiffer and Dörfler (22) for AC MGs to control power and frequency, stability, and frequency restoration. Tegling and Sandberg (23) discussed on distributed proportional-integral (PI) and proportional derivative (PD) controllers. These controllers can significantly improve voltage adjustment performance by a consensus protocol in double-integrator networks. The transient performance of DAPI is also compared with a droop controller by Andreasson et al. (24) for a multi-terminal high-voltage DC grid. The results obtained validate that the expected deviations from nominal voltages using the DAPI method are less than those obtained in the droop-controlled mode. However, there is less research focusing on implementing this method in DC MGs. Lee et al. (25) employed a consensus distributed-based load sharing for DC MG by considering the identical per-unit current of each converter, which is based solely on a proportional controller. In addition to the voltage and current regulations, the presence of CPLs poses certain challenges, particularly stability issues (26, 27). The presence of CPLs is studied in numerous literature sources (28, 29), and the compensation methods are also surveyed and reviewed (30, 31). Most of the research studies focus on controlling the buck converter of CPL.

The primary contribution of the presented paper is to introduce a DAPI controller for controlling a low-voltage

DC MG, which has not been considered before. This controller can achieve a good balance between voltage restoration and current sharing without relying on a central controller and with limited low-bandwidth communication links. This strategy is model-free because there is no need to know the MG's topology. Given that the presence of Constant Power Loads (CPLs) poses a challenge in DC MGs, a virtual control loop is incorporated into the suggested secondary controller of the reference DG. This control loop is based on the output voltage of CPL as a correction term to mitigate instability in the DC MG.

The rest of this paper covers the following issues. Section 2 describes the conventional droop method and introduces the DAPI secondary controller. The studied DC MG and results provided by implementing the proposed method are illustrated in section 3. Eventually, section 4 concludes the paper.

2. THE PROPOSED CONTROLLER

Most of the literature discusses the implementation of a decentralized strategy for power sharing and voltage regulation. Occasionally, the droop method is considered a strategy in DC microgrids. However, a secondary controller is being considered due to some setbacks of the droop method. In this research, a distributed-based controller is designed and integrated into the droop strategy to address its limitations. This section first explains the droop method, followed by a detailed description of the proposed secondary controller in the following subsections.

2. 1. Primary Droop Based Controller In the traditional droop strategy, the reference voltage can be mathematically expressed as follows based on the output current (32):

$$v_i = V_i^{ref} - r_i . I_i \quad (1)$$

where V_i^{ref}, r_i, v_i, and I_i are the rated voltage value, droop coefficient, and output voltage and current values, respectively. It is necessary that v_i tracks V_i^{ref} well.

On the other hand, the voltage of the bus for multi-paralleled DGs in a DC microgrid can be given as:

$$V_{bus} = v_i - R_i . I_i \quad (2)$$

where V_{bus} and R_i are the voltage of the bus and resistance of the line, respectively. Considering both Equations 1 and 2, the following equation can be written.

$$V_{bus} = V_i^{ref} - (R_i + r_i) . I_i \quad (3)$$

That means:

$$(R_i + r_i) . I_i = (R_k + r_k) . I_k \ , \ \forall i,k \quad (4)$$

It is clearly observed that $(R_i + r_i)$ is inversely proportional to current sharing, i.e. $I_i / I_k = (R_k + r_k)/(R_i + r_i), \ \forall i,k$. Considering $r_i \gg R_i$, we have:

$$\frac{I_i}{I_k} \simeq \frac{r_k}{r_i} \ , \ \forall i,k \quad (5)$$

It can be seen that r_i dominates the current sharing. Notably, the larger r_i results in better current sharing and worse voltage regulation, and vice versa. Consequently, r_i is designed by considering a tradeoff between power sharing and voltage restoration. The droop-based primary controller schematic is illustrated in Figure 1.

2. 2. Proposed Distributed Secondary Controller Even r_i is designed well based on equations, errors in current sharing and voltage restoration can be observed. In order to restore voltage to its nominal value and accurately share power, a DAPI controller is considered.

To design the DAPI controller, Equation 1 can be considered as:

$$v_i = V_i^{ref} - r_i . I_i + \vartheta_i \quad (6)$$

where ϑ_i is the generated signal by the secondary controller. Any delay in the output voltage adjustment

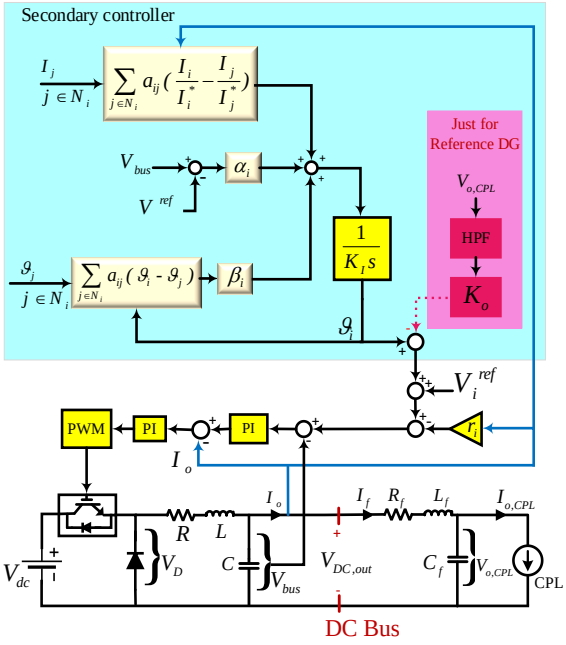


Figure 1. The structure of droop based primary controller and proposed DAPI-based secondary controller

can be tackled by passing through a low-pass filter, preventing unnecessary technical complications. Assuming these considerations yields Equation 6 to be written as below in vector notation.

$$v = -\left(v - V_i^{ref}\right) - r \,.\, I + \vartheta \tag{7}$$

where v, V_i^{ref}, and ϑ are voltage amplitude, reference voltage, and secondary control input vectors. Based on the theorem stated by Tegling and Sandberg (23) for the DAPI controller, as we can consider Equation 8 for v_i, the integral state for the secondary control input, ϑ, can be expressed as Equation 9.

$$u_i = -\sum_{n\in N_i} f_{ij}\left(x_i - x_j\right) - \sum_{n\in N_i} g_{ij}\left(v_i - v_j\right) - g_0 v_i + K_I z_i \tag{8}$$

$$\dot{z}_i = -v_i - \sum_{n\in N_i} c_{ij}\left(z_i - z_j\right) \tag{9}$$

In the above equations, z_i shows the integral state; K_I denotes the integral gain; and f_{ij}, g_{ij}, and g_0 are positive gains (23).

Considering Equation 9 along with the total secondary error as Equation 10, and combining with Equations 8 and 9; Equation 11 can be consequently defined for ϑ in this paper as the secondary control variable.

$$e_i = \alpha_i\left(V_{bus} - V_i^{ref}\right) + \beta_i\left(\sum_{n\in N_i} a_{ij}\left(\vartheta_i - \vartheta_j\right)\right) \tag{10}$$

$$K_I\dot{\vartheta} = -\alpha_i\left(V_{bus} - V_i^{ref}\right) - \beta_i\left(\sum_{n\in N_i} a_{ij}\left(\vartheta_i - \vartheta_j\right)\right) - \sum_{n\in N_i} a_{ij}\left(\frac{I_i}{I_i^*} - \frac{I_j}{I_j^*}\right) \tag{11}$$

where α_i and β_i are positive gains; and a_{ij} denotes the weight of the edge between the ith and jth buses. It is worth mentioning that $\vartheta = \left(k_p + \frac{k_i}{s}\right)e_i$. The overall diagram can be observed in Figure 1 (For more details on the DAPI based controllers (23)).

2. 3. Considering CPL According to the voltage-current ($V-I$) curve of a resistive load, the current varies proportional to the voltage. However, all of the loads are not resistive. If a resistive load (R_{Load}) is connected to the grid by a buck converter, the aggregation of R_{Load} and buck converter, depicted in Figure 2, is assumed as a CPL. Indeed, since the buck converter maintains the output voltage constant, it results in fixed consumed power of the resistive load.

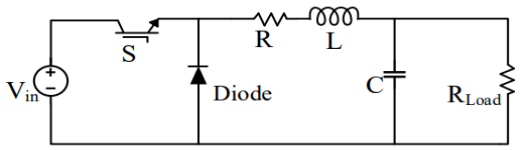


Figure 2. The aggregation of RL load and buck converter as a CPL from V_{in}'s side

The power of CPL provided by voltage and current is constant. Thus, based on Figure 3(a), if the voltage increases/decreases, the current decreases/increases, which leads to instability. According to Figure 3(a), the instantaneous resistance is positive ($V/I>0$), and the small signal resistance is negative ($dV/dI<0$). As a result, this negative resistance can impact power quality issues as well as the stability of the system (33).

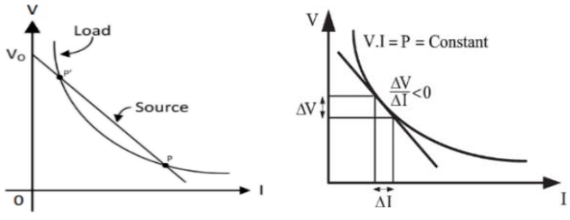
Figure 3(b) shows the instability resulting from the negative resistance. At the point P, the slope of $V-I$ curve of the source is bigger than that of CPL, which means that even though the small signal resistance is negative, its absolute value is smaller than the source's resistance; thus, P is unstable. Conversely, the slope of the CPL curve at P' is negative and its absolute value is bigger than the source's resistance, and thus, P' is stable.

Consequently, an investigation of the stability condition of CPLs is required. To do so, the following equations can be derived according to considering Figure 4.

$$\begin{cases} i = \dfrac{P}{v} \\ L\dfrac{di_L}{dt} = v_{dc} - R\,i_L - v \\ C\dfrac{dv_0}{dt} = i_L - i \end{cases} \tag{12}$$

By linearizing Equation 12 around the operational point, we have:

$$\begin{cases} \Delta i = \dfrac{P_0}{v_0^2}\Delta v \\ \dfrac{d\Delta i_L}{dt} = \dfrac{1}{L}\Delta v_{dc} - \dfrac{R}{L}\Delta i_L - \dfrac{1}{L}\Delta v \\ \dfrac{d\Delta v}{dt} = \dfrac{1}{C}\Delta i_L - \dfrac{1}{C}\Delta i \end{cases} \tag{13}$$



(a) (b)

Figure 3. (a) The *V-I* curve of CPL, (b) The *V-I* curve of CPL and source

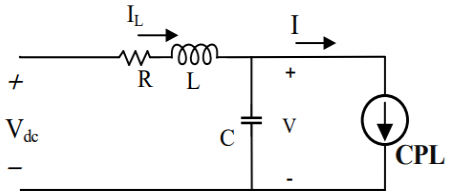


Figure 4. The CPL model with input LC filter

where the index of " 0 " is the operational point and " Δ " shows the changes around P_0. By simplification of Equation 13,

$$\begin{cases} \frac{d\Delta i_L}{dt} = \frac{1}{L}\Delta v_{dc} - \frac{R}{L}\Delta i_L - \frac{1}{L}\Delta v \\ \frac{d\Delta v}{dt} = \frac{1}{C}\Delta i_L - \frac{P_0}{Cv_0^2}\Delta i \end{cases} \quad (14)$$

Based on Equation 14, the characteristic equation of the system is derived as:

$$s^2 + s\left(\frac{R}{L} - \frac{P_0}{Cv_0^2}\right) + \left(\frac{1}{LC} - \frac{P_0 R}{LCv_0^2}\right) = 0 \quad (15)$$

Based on Equation 15, two conditions are required to have a stable system as the following:

$$\begin{cases} \frac{R}{L} > \frac{P_0}{Cv_0^2} \Rightarrow \frac{R}{L} > \frac{1}{rC} \\ \frac{v_0^2}{P_0} > R \Rightarrow \frac{1}{R} > \frac{1}{r} \end{cases} \quad (16)$$

The above conditions are stability conditions, although the first condition typically encompasses the second one. It is clear that changing the CPL, the input filter to ensure stability (34).

In literature, various methods are introduced mitigate for the negative effects CPLs, which are mainly categorized as passive and active methods. The former introduces a passive element to the output LC filter of the converter, which corrects the filter values and ensures stability. The latter employs methods such as feedback stabilizers, control loops, and virtual impedances to maintain stability. Active methods demonstrate higher efficiency, lower costs, and greater reliability due to the absence of passive and physical elements and the sole utilization of control loops (35, 36). An active strategy based on a feedback stabilizer is implemented here.

First, it should be mentioned that the feedback stabilizers are considered in two voltage and current modes and are also added to the system in three ways demonstrated in Figure 5. In these figures, R_{v0}, K_v, and R_{vi} are virtual resistances in current feedback mode; and in voltage feedback mode, K_0, K_{in}, and K_i are virtual variable coefficients; and there is a high pass filter as $G_{HPF}(S) = \frac{s}{s+\omega}$.

As illustrated in Figure 5, these feedback loops are considered in their primary controller. However, this paper adds these loops in just the secondary controller of the reference DG, which is depicted in Figure 1. Concerning the added feedback stabilizer to the control system, we first obtain the transfer function of the output impedance of the source ($Z_o(s)$), and then, we analyze the system's stability (equations are related to considering CPL). It should be mentioned that the voltage feedback is studied here, but the current one is the same, so we skip it. According to the circuit shown in Figure 1, we have:

$$\begin{cases} V_D = R\,I + Ls\,I + V_{Bus} \\ Cs\,V_{Bus} = I - I_o \end{cases} \quad (17)$$

Based on the control loop, we also have:

$$\begin{cases} I^* = G_V\left(V_{Bus}^* - V_{Bus}\right) \\ V_{Bus}^* = V^* - \boldsymbol{G_{HPF} K_0 V_{o,CPL}} \\ V_D = G_I\left(I^* - I\right) \end{cases} \quad (18)$$

With the linearization of Equations 17 and 18, the small signal model can be derived as:

$$\begin{cases} \tilde{V}_D = R\,\tilde{I} + Ls\,\tilde{I} + \tilde{V}_{Bus} \\ Cs\,\tilde{V}_{Bus} = \tilde{I} - \tilde{I}_o \end{cases} \quad (19)$$

$$\begin{cases} \tilde{I}^* = G_V\left(-\tilde{V}_{Bus} - \boldsymbol{G_{HPF} K_0 \tilde{V}_{o,CPL}}\right) \\ \tilde{V}_D = G_I\left(\tilde{I}^* - \tilde{I}\right) \end{cases} \quad (20)$$

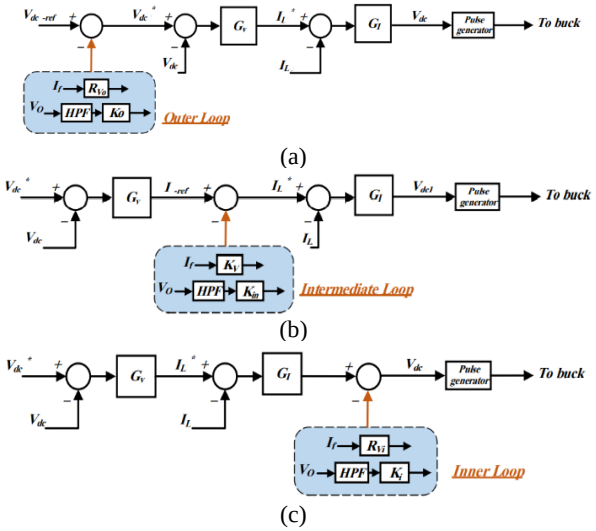


Figure 5. Control of buck with stabilizer virtual loops, (a) The outer one, (b) The middle one, (c) The inner one

By Equations 19 and 20, the following equation is obtained:

$$\begin{aligned} -G_I G_V \tilde{V}_{Bus} - G_I G_V G_{HPF} K_0 \tilde{V}_{o,CPL} - \\ G_I \tilde{I}^* = R\tilde{I} + Ls\tilde{I} + \tilde{V}_{Bus} \end{aligned} \quad (21)$$

In order to obtain $Z_{o,DC}$ which is the total impedance of the DC link, all of the variables should be defined based on $V_{DC,out}$ and I_o. Thus,

$$\begin{cases} \tilde{I} = Cs\,\tilde{V}_{Bus} + \tilde{I}_{Line} \\ \tilde{V}_{Bus} = R_{Line}\,\tilde{I}_o + L_{Line} s\,\tilde{I}_o + \tilde{V}_{DC,out} \end{cases} \quad (22)$$

Also, we have:

$$\tilde{I}_f = \tilde{I}_o = C_{f,CPL} s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \quad (23)$$

Then,

$$\begin{aligned} & G_I G_V \left(\begin{array}{l} R_{Line}\left(C_{f,CPL} s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) \\ \quad + L_{Line}\, s \left(C_{f,CPL}\, s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) + \tilde{V}_{o,CPL} \end{array} \right) \\ & - G_I \left(Cs \left(\begin{array}{l} R_{Line}\left(C_{f,CPL}\, s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) \\ \quad + L_{Line}\, s \left(C_{f,CPL}\, s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) + \tilde{V}_{o,CPL} \end{array} \right) \right) \\ & + \left(\begin{array}{l} R_{Line}\left(C_{f,CPL}\, s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) + \\ \quad L_{Line} s \left(\left(C_{f,CPL}\, s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) + \tilde{V}_{o,CPL} \right) \end{array} \right) \\ & = R \left(Cs \left(\begin{array}{l} R_{Line}\left(C_{f,CPL}\, s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) + \\ \quad L_{Line} s \left(\left(C_{f,CPL}\, s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) + \tilde{V}_{o,CPL} \right) \end{array} \right) \right) \\ & + Ls \left(Cs \left(\begin{array}{l} R_{Line}\left(C_{f,CPL} s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) \\ \quad + L_{Line} s \left(\left(C_{f,CPL} s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) + \tilde{V}_{o,CPL} \right) \end{array} \right) \right) \\ & + \left(\begin{array}{l} R_{Line}\left(C_{f,CPL} s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) + \\ \quad L_{Line} s \left(\left(C_{f,CPL} s\tilde{V}_{o,CPL} + \tilde{I}_{o,CPL} \right) + \tilde{V}_{o,CPL} \right) \end{array} \right) \\ & - G_I G_V G_{HPF} K_0 \tilde{V}_{o,CPL} \end{aligned} \quad (24)$$

Eventually, the total output impedance (Z_o) in existence of CPL can be written as:

$$\begin{aligned} Z_o = \frac{\tilde{V}_{o,CPL}}{\tilde{I}_{o,CPL}} = \\ \frac{\left(\begin{array}{l} \left(C\,L\,L_{Line} \right) s^3 + \left(G_I\, C\, L_{Line} + C\, L_{Line}\, R + C\, L\, R_{Line} \right) s^2 \\ + \left(G_I\, G_V\, L_{Line} + G_I\, C\, R_{Line} + C\, R\, R_{Line} + L + L_{Line} \right) s \\ + \left(G_I\, G_V\, R_{Line} + GI + R + R_{Line} \right) \end{array} \right)}{\left(\begin{array}{l} \left(C\, C_{f,CPL}\, L\, L_{Line} \right) s^4 + \\ \left(\begin{array}{l} G_I\, C\, C_{f,CPL}\, L_{Line} + C C_{f,CPL}\, L_{Line}\, R \\ \quad + C\, C_{f,CPL}\, L\, R_{Line} \end{array} \right) s^3 + \\ \left(\begin{array}{l} G_I\, G_V\, C_{f,CPL}\, L_{Line} + G_I\, C\, C_{f,CPL}\, R_{Line} \\ \quad + C\, C_{f,CPL}\, R\, R_{Line} + C\, L + C_{f,CPL}\, L_{Line} \end{array} \right) s^2 \\ + \left(\begin{array}{l} G_I\, G_V\, C_{f,CPL}\, R_{Line} + G_I\, C \\ \quad + G_I C_{f,CPL} + C\, R + C_{f,CPL}\, R_{Line} \end{array} \right) s + \\ + \left(G_I\, G_V + 1 + G_I G_V G_{HPF} K_0 \right) \end{array} \right)} \end{aligned} \quad (25)$$

Based on obtained Z_o, when CPL does not exist in the grid, there is no pole on the right side of the axis; therefore, the system is stable. However, adding CPL leads to the movement of poles to the right side. When the feedback stabilizers are considered as the above equations, the system's stability depends on changes in K_o and ω of HPF. Figures 6(a) and 6(b) show the pole locus investigations by changing these parameters.

As evident from Figure 6, when these parameters are increased, the system's poles move to the left side, and as a result, the system remains stable. Thus, the system can be stable without adding any passive elements and merely with virtual control loops in the proposed secondary controller. It is worth mentioning that K=0 and a frequency of *100 Hz* are considered here.

3. RESULTS AND DISCUSSION

To verify the performance of the proposed scheme, a DC MG is studied and simulated using MATLAB/Simulink software. This MG is illustrated in Figure 7 and operates in islanded mode. The nominal voltage of the MG is 48 V, and there are two 500 W loads. Four DGs are integrated into the studied MG, and each DG is connected to the grid by a DC/DC buck converter. The data of the DGs and other required information are provided in Table 1. The forthcoming scenarios will be thoroughly verified and compared with the results obtained by other methods reported in literature (21, 29):

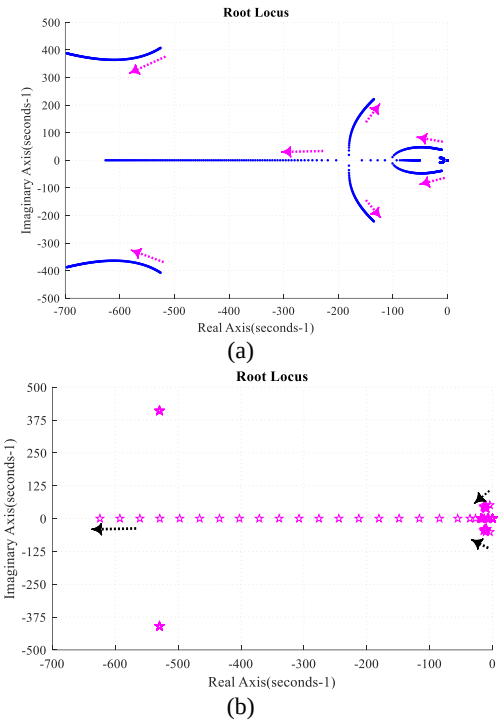


Figure 6. (a) Increase in K_o from 0 to 2.5 and constant value of 100 for frequency of HPF, (b) Increase in frequency of HPF from 0 to 200 and K_o = 1

- ***Case I***: The grid is just controlled by the primary droop controller.
- ***Case II***: The proposed DAPI secondary controller is activated at *t= 2 s*.
- ***Case III***: A CPL (with a constant power of *320 W*) is added to loads at *t = 4 s*.
- ***Case IV***: At *t=5.5 s*, the link between DG_2 and DG_3 is disconnected and connected again a *t=7 s*.
- ***Case V***: DG_4 is considered to be the backup unit that can be disconnected and connected. Plugging out is occurred at *t= 8.5 s*, and at *t =4.5 s*, it is plugged in.

It is worth noting that to implement the secondary controller, a graph is considered for the demonstration of DG communication links. The following adjacency matrix is considered here.

$$A=\begin{bmatrix}0&1&0&1\\1&0&1&0\\0&1&0&1\\1&0&1&0\end{bmatrix} \quad (26)$$

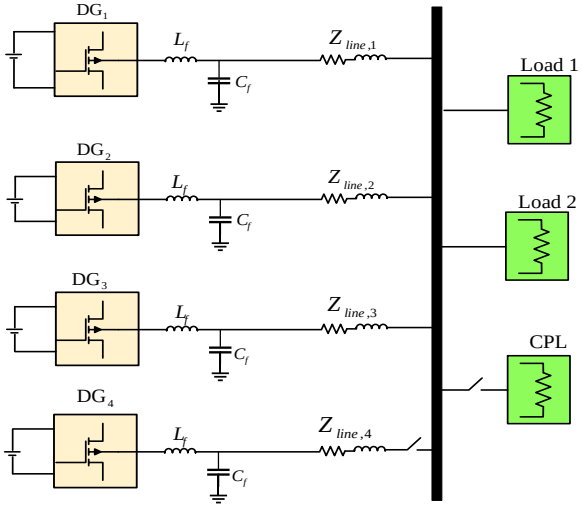


Figure 7. Diagram of the studied DG MG

TABLE 1. Parameters of the DC MG

Symbol	Quantity	DG_1 & DG_2	DG_3 & DG_4
V_i^{ref}	nominal DC voltage	48 V	48 V
ΔV	allowable deviation	5%	5%
V_{dc}	voltage source	100 V	100 V
L	filter inductance	1.5 mH	1.5 mH
C	filter capacitance	470 μF	470 μF
$k_P - k_I$	voltage controller	0.1-1	0.1-1
$k_P - k_I$	current controller	0.01-1	0.01-1
r	droop coefficient	1.2 V/W	0.8 V/W
Secondary controller parameters			
K_I	Integrator gain	1	1
α	Combination gain	1	1
β	Combination gain	1	1

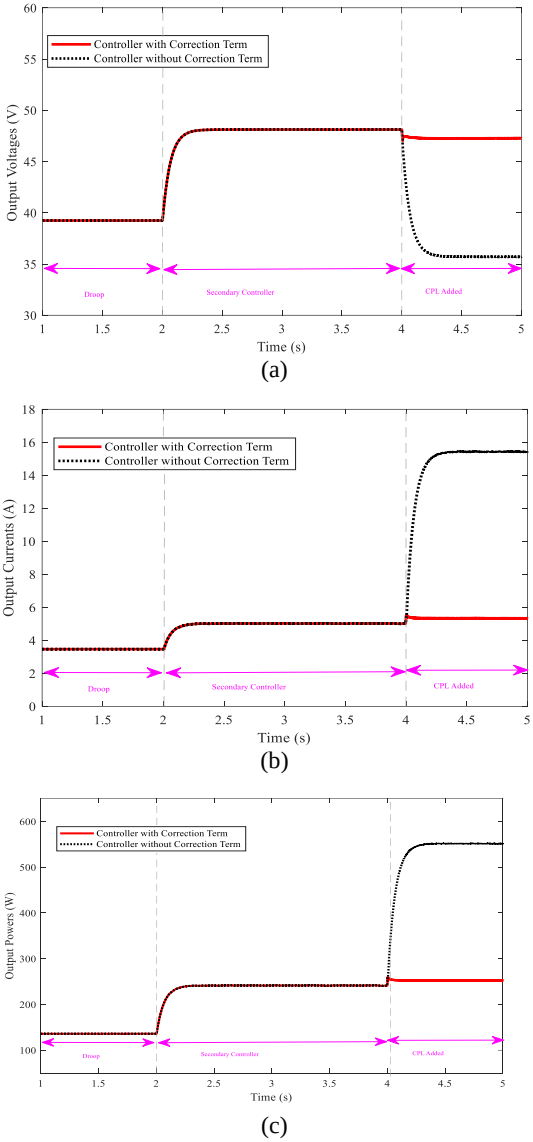


Figure 8. (a) Output voltage, (b) Output current, (c) Output power obtained by the proposed method

The activation of the proposed secondary controller is compared for two cases: considering and ignoring the virtual loop. The results are illustrated for DG2 in Figure 8. It is evident that when the secondary controller is activated, the voltage is restored to its nominal value of

48 V (Figure 8(a)), and the current and power are shared proportionally (Figures 8(b) and 8(c)). While adding CPL at t=4 s, considering the proposed virtual loop for the reference DG (DG1 in this case) results in a negligible voltage drop of 3 V. However, neglecting this loop causes a significant voltage drop, posing a threat of instability. Therefore, it can be said that based on Figure 8, considering the feedback of CPL's voltage in the secondary controller prevents instability and ensures better performance of the controller.

To provide a more meaningful comparison and demonstrate the superior performance of the proposed controller, the results obtained from implementing the proposed strategy and the strategy proposed by Xing et al. (21) are depicted in Figures 9 and 10. The primary

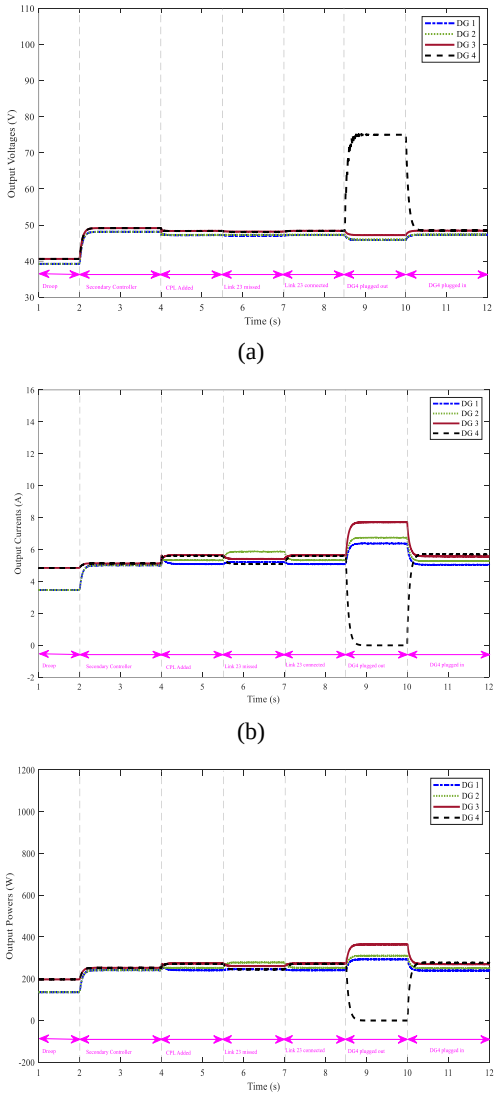


Figure 9. (a) Output voltage, (b) Output current, (c) Output power obtained by the proposed method

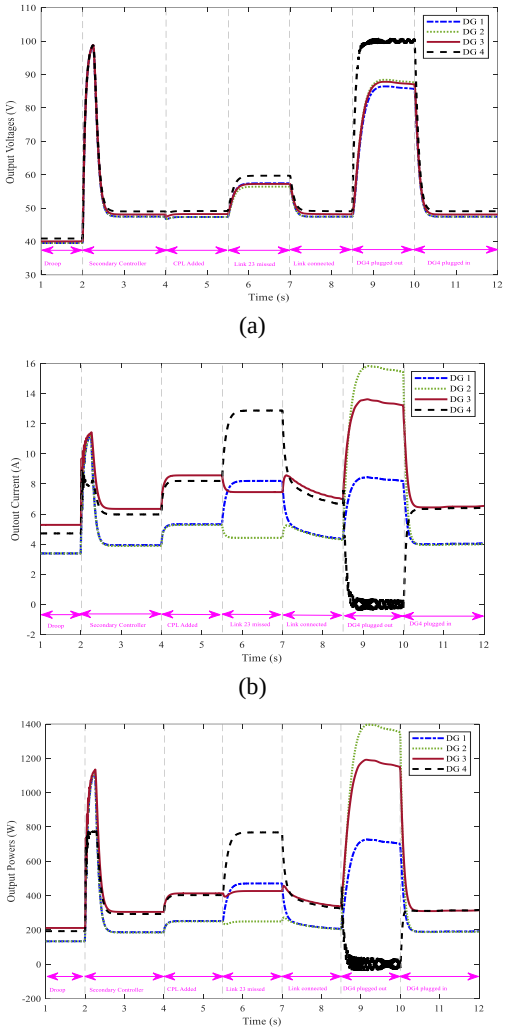


Figure 10. (a) Output voltage,(b) Output current, (c) Output power obtained by the proposed method of [21]

control is initially activated. From Figures 9 (a) and 9(b), the output voltages decrease to about 40 V. Once the proposed secondary control is implemented, the output voltages are restored to their nominal value. Our proposed method exhibits no overshoot when the secondary controller is implemented, whereas the approach by Xing et al. (21) showed a significant overshoot. Moreover, despite the slow convergence in results obtained by the method proposed by Xing et al. (21), the absence of overshoot in the proposed method results in rapid convergence and earlier voltage stabilization. As far as Figures 9(b) and 10(b), which show the current sharing, and Figures 9(c) and 10(c), which illustrate the power-sharing, are concerned, it is evident that the proposed method outperforms the method presented by Dam and Lee (20). Having a more comprehensive comparison between the proposed

method in this paper and that of by Xing et al. (21), the voltage and power errors of DG4 are presented in Table 2. This table shows the following cases: 1) Secondary controller, 2) Adding CPL, 3) After link restoration, and 4) After DG plugged in.

Based on the results presented in Table 2, it is evident that our proposed method outperforms the others, demonstrating higher accuracy in voltage adjustment and power sharing. In case 1, which involves the activation of the secondary controller, the voltage error and power error percentages of DG2 are 0% and 1.5% consecutively according to the proposed method. In comparison, they are 2.08% and 12.5% for the method proposed by Xing et al. (21), respectively. The validation of the proposed method is also compared to other schemes, with the strategy proposed by Hassan et al. (29) being considered. The errors are also calculated, and the mentioned values are obtained as 1.97% and 9.94% for the method (29). The method presented here achieves the precise reference voltage. For case 2, the CPL is added, and the voltage error percentages obtained by the proposed method and the methods of Xing et al. (21) and Hassan et al. (29) are 0.83%, 2.39%, and 3.13%, respectively. The power errors are 15.38% for our method, 55% for Xing et al. (21), and 56.3% for Hassan et al. (29). These results illustrate better performance in power-sharing achieved by the proposed strategy. In case 3, where errors are calculated after the link restoration between DG2 and DG3, the voltage and power errors of our strategy are 0.83% and 15.38%, respectively. In comparison, they are 2.5% and 21.15% for the strategy proposed by Xinget al. (21), and 3.39% and 23.8% for the strategy proposed by Hassan et al. (29), demonstrating better performance. Moreover, in case 4, which displays the values after the reconnection of DG4, the voltage errors are 1.6%, 2.5%, and 3.26% for the proposed method and the methods of Xinget al. (21) and Hassan et al. (29), indicating superior voltage adjustment. The power errors are 19.6%, 23.07%, and 19.87%, showcasing significantly improved results of the proposed method for power allocation in play mode. It is worth mentioning that if the voltage and power errors are calculated for the link disconnection case and DG4 plug-and-play mode, the proposed method can perform adequately. The errors are significantly lower compared to the errors in the methods proposed by Xing et al. (21) and Hassan et al. (29), indicating that the proposed method operates effectively. In addition, the convergence speed for achieving a stable condition after any changes in topology or communication links is evident in all figures.

TABLE 2. Voltage and Power Error Percentages of DG_4

e_v				
Cases	**1**	**2**	**3**	**4**
Proposed Method	0%	0.83%	0.83%	1.6%
Method of Xing et al. [21]	2.08%	2.39%	2.5%	2.5%
Method of [29]	1.97%	3.13%	3.39%	3.26%
e_p				
Proposed Method	1.5%	15.38%	15.38%	19.6%
Method of [21]	12.5%	55%	21.15%	23.07%
Method of [29]	9.94%	56.3%	23.8%	19.87%

4. CONCLUSION

A DAPI secondary control strategy was introduced in this paper for islanded DC MGs to allocate power and adjust voltage. This strategy also included a virtual control loop based on the output voltage of CPL. Like most literature, the primary layer was controlled by a droop controller, while the secondary level was influenced by a feedback strategy, in contrast to other existing feed-forward secondary control strategies. This DAPI controller requires sparse communication among neighboring DGs and utilizes decentralized control actions to regulate voltage precisely and share current appropriately. The effectiveness of this method was confirmed by applying it in an islanded DC MG, consisting of 4 DGs, regular loads, and CPL, and comparing it with another existing strategy. The results obtained from the simulation showed better convergence, no overshoot, and more accurate adjustments of the proposed method. In addition, the stability of DC MG was guaranteed by considering the virtual control loop in the presence of CPL.

5. REFERENCES

1. Khanalizadeh Eini M, Mirhosseini Moghadam M, Tavakoli A, Alizadeh B. Stability analysis of ac/dc microgrids in island mode. International Journal of Engineering, Transactions A: Basics. 2021;34(7):1750-65. 10.5829/IJE.2021.34.07A.20
2. Justo JJ, Mwasilu F, Lee J, Jung J-W. AC-microgrids versus DC-microgrids with distributed energy resources: A review. Renewable and sustainable energy reviews. 2013;24:387-405. https://doi.org/10.1016/j.rser.2013.03.067
3. Zare H, Khanalizadeh Eini M, Esmaeili A. Stabilization of Voltage and Current in the Distribution Networks using APF and TSC. International Journal of Engineering, Transactions B: Applications. 2022;35(5):1064-73. 10.5829/ije.2022.35.05b.21
4. Dragičević T, Lu X, Vasquez JC, Guerrero JM. DC microgrids—Part II: A review of power architectures, applications, and standardization issues. IEEE transactions on power electronics. 2015;31(5):3528-49. 10.1109/TPEL.2015.2464277
5. Espina E, Llanos J, Burgos-Mellado C, Cardenas-Dobson R, Martinez-Gomez M, Saez D. Distributed control strategies for microgrids: An overview. IEEE Access. 2020;8:193412-48. 10.1109/ACCESS.2020.3032378
6. Gao F, Gu Y, Bozhko S, Asher G, Wheeler P, editors. Analysis of droop control methods in DC microgrid. 2014 16th European

Conference on Power Electronics and Applications; 2014: IEEE. 10.1109/EPE.2014.6910846

7. Liu Y, Han Y, Lin C, Yang P, Wang C, editors. Design and implementation of droop control strategy for DC microgrid based on multiple DC/DC converters. 2019 IEEE innovative smart grid technologies-Asia (ISGT Asia); 2019: IEEE. 10.1109/ISGT-Asia.2019.8881129
8. Dehaghania MN, Biglarahmadia M, Mousavi SM, Abdolahic M. A Distributed Cooperative Secondary Control Scheme for Obtaining Power and Voltage References of Distributed Generations in Islanded DC Microgrids. International Journal of Engineering, Transactions B: Applications. 2024;37(02):341. 10.5829/IJE.2024.37.02B.10
9. Meng L, Dragicevic T, Roldán-Pérez J, Vasquez JC, Guerrero JM. Modeling and sensitivity study of consensus algorithm-based distributed hierarchical control for DC microgrids. IEEE Transactions on Smart Grid. 2015;7(3):1504-15. 10.1109/TSG.2015.2422714
10. Dou C, Yue D, Zhang Z, Ma K. MAS-based distributed cooperative control for DC microgrid through switching topology communication network with time-varying delays. IEEE Systems Journal. 2017;13(1):615-24. 10.1109/JSYST.2017.2726081
11. Khanalizadeh Eini M, Mirhosseini Moghadam M, Tavakoli A, Alizadeh B. Stability analysis of ac/dc microgrids in island mode. International Journal of Engineering. 2021;34(7):1750-65. 10.5829/IJE.2021.34.07A.20
12. Mathew P, Madichetty S, Mishra S. A multilevel distributed hybrid control scheme for islanded DC microgrids. IEEE Systems Journal. 2019;13(4):4200-7. 10.1109/JSYST.2019.2896927
13. Biglarahmadi M, Ketabi A, Baghaee HR, Guerrero JM. Integrated nonlinear hierarchical control and management of hybrid AC/DC microgrids. IEEE Systems Journal. 2021;16(1):902-13. 10.1109/JSYST.2021.3050334
14. Nabian Dehaghani M, Taher SA, Dehghani Arani Z. An efficient power sharing approach in islanded hybrid AC/DC microgrid based on cooperative secondary control. International Transactions on Electrical Energy Systems. 2021;31(6):e12897. https://doi.org/10.1002/2050-7038.12897
15. Dehaghani MN, Taher SA, Arani ZD, editors. Distributed Secondary Voltage and Current Control Scheme with Noise Nullification Ability for DC Microgrids. 2020 10th Smart Grid Conference (SGC); 2020: IEEE. 10.1109/SGC52076.2020.9335768
16. Li Y, Zhang Z, Dragičević T, Rodriguez J. A unified distributed cooperative control of DC microgrids using consensus protocol. IEEE Transactions on Smart Grid. 2020;12(3):1880-92. 10.1109/TSG.2020.3041378
17. Morstyn T, Hredzak B, Demetriades GD, Agelidis VG. Unified distributed control for DC microgrid operating modes. IEEE Transactions on Power Systems. 2015;31(1):802-12. 10.1109/TPWRS.2015.2406871
18. Guo F, Xu Q, Wen C, Wang L, Wang P. Distributed secondary control for power allocation and voltage restoration in islanded DC microgrids. IEEE Transactions on Sustainable Energy. 2018;9(4):1857-69. 10.1109/TSTE.2018.2816944
19. Sahoo S, Mishra S. A distributed finite-time secondary average voltage regulation and current sharing controller for DC microgrids. IEEE Transactions on Smart Grid. 2017;10(1):282-92. 10.1109/TSG.2017.2737938
20. Dam D-H, Lee H-H. A power distributed control method for proportional load power sharing and bus voltage restoration in a DC microgrid. IEEE transactions on industry applications. 2018;54(4):3616-25. 10.1109/TIA.2018.2815661
21. Xing L, Mishra Y, Guo F, Lin P, Yang Y, Ledwich G, et al. Distributed secondary control for current sharing and voltage restoration in DC microgrid. IEEE Transactions on Smart Grid. 2019;11(3):2487-97. 10.1109/TSG.2019.2956515
22. Schiffer J, Dörfler F, editors. On stability of a distributed averaging PI frequency and active power controlled differential-algebraic power system model. 2016 European Control Conference (ECC); 2016: IEEE. 10.1109/ECC.2016.7810500
23. Tegling E, Sandberg H. On the coherence of large-scale networks with distributed PI and PD control. IEEE control systems letters. 2017;1(1):170-5. 10.1109/LCSYS.2017.2711781
24. Andreasson M, Tegling E, Sandberg H, Johansson KH, editors. Performance and scalability of voltage controllers in multi-terminal HVDC networks. 2017 American Control Conference (ACC); 2017: IEEE. 10.23919/ACC.2017.7963412
25. Lee J, Kim B, Back J, editors. A distributed proportional load sharing controller for dc microgrids. 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019-ECCE Asia); 2019: IEEE. 10.23919/ICPE2019-ECCEAsia42246.2019.8797036
26. AL-Nussairi MK, Bayindir R, Padmanaban S, Mihet-Popa L, Siano P. Constant power loads (cpl) with microgrids: Problem definition, stability analysis and compensation techniques. Energies. 2017;10(10):1656. https://doi.org/10.3390/en10101656
27. Murtaza SA, Siddique N, Aslam J, Latif W, Wasif M, Hussain I. Improving the stability of islanded DC microgrid with constant power loads. Engineering Proceedings. 2022;12(1):11. https://doi.org/10.3390/engproc2021012011
28. Sadabadi MS, Shafiee Q. Scalable robust voltage control of DC microgrids with uncertain constant power loads. IEEE Transactions on Power Systems. 2019;35(1):508-15. 10.1109/TPWRS.2019.2928512
29. Hassan MA, Su C-L, Chen F-Z, Lo K-Y. Adaptive passivity-based control of a DC–DC boost power converter supplying constant power and constant voltage loads. IEEE Transactions on Industrial Electronics. 2021;69(6):6204-14. 10.1109/TIE.2021.3086723
30. Hossain E, Perez R, Nasiri A, Padmanaban S. A comprehensive review on constant power loads compensation techniques. IEEE access. 2018;6:33285-305. 10.1109/ACCESS.2018.2849065
31. Hassan MA, Su C-L, Pou J, Sulligoi G, Almakhles D, Bosich D, et al. DC shipboard microgrids with constant power loads: A review of advanced nonlinear control strategies and stabilization techniques. IEEE Transactions on Smart Grid. 2022;13(5):3422-38. 10.1109/TSG.2022.3168267
32. Huang P-H, Liu P-C, Xiao W, El Moursi MS. A novel droop-based average voltage sharing control strategy for DC microgrids. IEEE transactions on Smart Grid. 2014;6(3):1096-106. 10.1109/TSG.2014.2357179
33. Wu M, Lu DD-C. A novel stabilization method of LC input filter with constant power loads without load performance compromise in DC microgrids. IEEE Transactions on industrial electronics. 2014;62(7):4552-62. 10.1109/TIE.2014.2367005
34. Sanchez S, Molinas M, editors. Assessment of a stability analysis tool for constant power loads in DC-grids. 2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC); 2012: IEEE. 10.1109/EPEPEMC.2012.6397317
35. Shafiee Q, Dragicevic T, Vasquez JC, Guerrero JM, editors. Modeling, stability analysis and active stabilization of multiple DC-microgrid clusters. 2014 IEEE international energy conference (ENERGYCON); 2014: IEEE. 10.1109/ENERGYCON.2014.6850588
36. Lu X, Sun K, Huang L, Guerrero JM, Vasquez JC, Xing Y, editors. Virtual impedance based stability improvement for DC microgrids with constant power loads. 2014 IEEE Energy Conversion Congress and Exposition (ECCE); 2014: IEEE. 10.1109/ECCE.2014.6953759

Persian Abstract

چکیده

توجه بیشتر به انرژی‌های تجدیدپذیر و پیشرفت در الکترونیک قدرت منجر به کاربرد بیشتر ریزشبکه‌های جریان مستقیم (DC MGs) شده است. با این حال، MGهای DC دارای چالش‌هایی نظیر تنظیم ولتاژ و تقسیم توان هستند. برای حل این مشکل، یک ساختار کنترل سلسله مراتبی دو لایه شامل یک استراتژی کنترل ثانویه کاملاً توزیع‌شده جدید و روش کنترل افتی اولیه مرسوم در این مقاله پیشنهاد و به کار گرفته شده است تا به طور دقیق توان را تقسیم کند و ولتاژ را به سرعت تنظیم کند. در واقع، یک استراتژی کنترل ثانویه انتگرالی تناسبی-انتگرالی توزیع‌شده (DAPI) معرفی شده است. مشکل دیگر درMG های DC، وجود بارهای توان ثابت (CPL) است که ممکن است منجر به ناپایداری شود. برای غلبه بر این مشکلات به وجود آمده از حضور CPL، ترمی مبتنی بر ولتاژ خروجی CPL به DAPI پیشنهادی اضافه می‌گردد که از ناپایداری جلوگیری می‌کند. با استفاده از داده‌های محلی شین DC و ورودی‌های کنترل ثانویه واحدهای مجاور، و با الهام از کنترل مشارکتی، ورودی‌های کنترل مورد نیاز به دست می‌آیند. علاوه‌براین، این استراتژی نیازی به دانستن توپولوژی ریزشبکه ندارد که انعطاف‌پذیری را افزایش می‌دهد. برای اعتبار سنجی استراتژی DAPI پیشنهادی در DC MGها، یک DC MG جزیره‌ای در نرم‌افزار MATLAB/SIMULINK شبیه‌سازی شده است. نتایج و مقایسه آنها با نتایج به‌دست‌آمده از روش موجود دیگر، عملکرد کنترل‌کننده DAPI پیشنهادی را در سناریوهای مختلفplug-and-play، قطع ارتباط و تغییرات بار اثبات می‌کند