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Gate Oxide Thickness and Drain Current Variation of Dual Gate Tunnel Field Effect Transistor

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Two-dimensional analytical modelling of Dual Material Gate Tunnel Field Effect Transistor with change in variation of gate oxide thickness (DMG-UOX-TFET) is proposed in this work. This proposed device employs dielectric materials such as hafnium oxide and silicon dioxide, with distinct oxide thicknesses. This device was invented using a technology-aided computer design tool in 10 nm (0.01 µm) technology. This work investigates the impact of gate oxide thickness on the electrical characteristics of the proposed device, with a particular focus on drain current variation. The extensive simulations and key performance parameters of the proposed device were analyzed regarding gate oxide thickness. The various gate oxide thicknesses and their effects on the device subthreshold slope, On- current, Off- current, and on-off-current ratio were analyzed. The proposed device incorporates n-type operations within the gate overlap region, effectively mitigating the corner effect and the detrimental band-to-band tunneling that can degrade the on/off ratio. Through careful optimization of the doping concentration in the gate overlap region, achieved a remarkable ~4.8 time enhancement in the on-current, while simultaneously reducing the average subthreshold swing from 91.3 mV/dec to 52.8 mV/dec.

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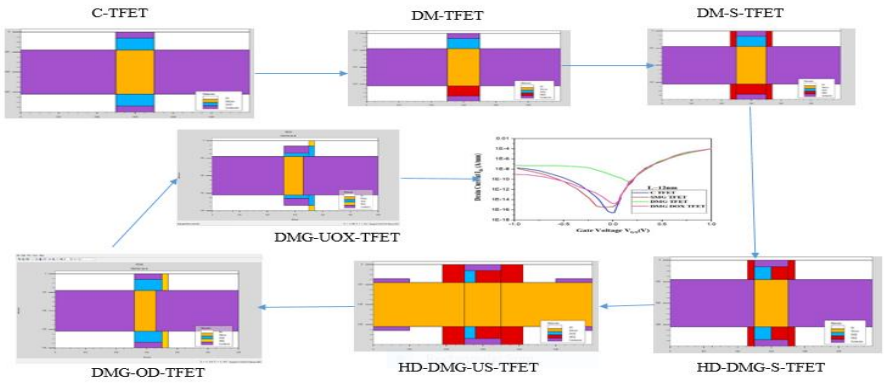
Graphical Abstract



NOMENCLATURE

N_d	Doping concentration	W_f	Gate work function
t_{si}	Thickness of silicon dioxide	*The*	Thickness of low k material
T_{hk}	Thickness of high k material	V_{gs}	Gate to source voltage
I_{on}	On state current (A/µm)	t_{ox}	Oxide thickness (nm)

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1. INTRODUCTION

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET), stands as one of the foundational building blocks of modern electronics. Since its invention in the 1960s, the MOSFET has played a pivotal role in revolutionizing the semiconductor industry and enabling the advanced research and rapid speed of technology growing. This versatile and highly adaptable transistor has become the cornerstone of integrated circuits, powering everything essential to have circuits with nanooptimized scaling area for circuit analysis and to operate with the high frequency processing speed concerning low power consumption (1). At its core, the MOSFET is a solid-state electronic device that controls the flow of electrical current through a semiconductor channel via an electric field generated by a gate electrode. Its unique operation is based on the principle characteristics of field-effect modulation, distinct from the bipolar junction transistor (BJT) and which relies on control the on current (2). This fundamental difference gives the MOSFET several advantages, including lower power consumption, fast switching speeds, and scalability for integration into densely packed semiconductor chips (3).

The heart of the MOSFET is its gate terminal, separated from the semiconductor channel by a thin insulating layer typically made of silicon dioxide (SiO_2). By applying a voltage to the gate, the MOSFET can either allow or block the flow of current between its sources and drain terminals (4). This voltage-controlled behavior makes it an ideal choice for digital logic and analog signal processing applications.The MOSFET structure has three terminals gate, source, and drain; which are in nm. The source is the terminal from which the current enters the device, while the drain is where it exits. The gate terminal controls the flow of current between the source and the drain (5).

The CMOS technology is a widely used implementation of MOSFETs. CMOS circuits consume minimal power when idle and are commonly found in digital logic and microprocessor designs. Over the years, MOSFETs have scaled down in size, following Moore's Law, which states that the number of transistors and size on a chip doubles approximately every two years. Smaller transistors allow for higher packing densities and improved performance. MOSFETs find applications in a vast array of electronic devices, including computers, smartphones, power amplifiers, voltage regulators, and more in low power. They are essential components in digital integrated circuits, leading to the miniaturization and increased efficiency of electronic systems (6).

The structure of Tunnel Field Effect Transistor (TFET) is an advanced semiconductor device in the industry that has gained significant attention in recent years for its potential performanc to overcome some of the limitations of traditional MOSFET over the semiconductor industry. TFETs operate on a fundamentally different principle, leveraging quantum mechanical tunneling effects to control the flow of charge through a semiconductor intrinsic channel (7). This unique operation makes them promising devices for various applications, including low-power electronics and high-frequency analog circuits. TFETs are continuous rely on the quantum tunneling phenomenon where charge carriers can pass through a thin insulating barrier even when they do not possess enough energy to overcome the barrier in classical physics. In TFETs, this tunneling occurs between the source and drain terminals through a thin channel region. One of the most significant advantages of TFETs is their ability to achieve subthreshold slopes much steeper than those of traditional MOSFETs (8). This results in extremely low leakage currents when the TFET is in the off-state, making them highly energy-efficient devices.

The TFETs are particularly well suited for low-power applications because they can operate at lower supply voltages and exhibit reduced off-state leakage current. This property makes them attractive for use in battery-powered devices and energy-efficient integrated circuits (9). The performance of TFETs is highly dependent on the choice of semiconductor materials and their bandgap characteristics. Materials with narrow bandgaps are often preferred for TFETs to enhance tunneling effects and improve device performance. TFETs have the potential to impact a wide range of applications, including digital logic circuits, low-power processors, radio-frequency amplifiers, and analog circuits (10). They are especially promising for Internet of Things devices, where energy efficiency is critical. Despite their promise, TFETs face challenges such as low on-state current, fabrication complexity, and sensitivity to process variations. Researchers are actively working to address these issues and unlock their full potential (11).

The Single Gate TFET (SG-TFET), is an emerging semiconductor device that has attracted considerable attention in recent years for its potential to address some of the energy efficiency and performance challenges faced by conventional transistors (12, 13). It is a type of TFET that operates based on quantum mechanical tunneling phenomena, offering a steep subthreshold slope and reduced power consumption. The SG-TFET has exploit quantum tunneling, a quantum mechanical phenomenon where charge carriers can pass through an energy barrier that they classically should not be able to overcome (14). This property allows SG-TFET to exhibit subthreshold slopes well below the fundamental limit of traditional transistors. SG-TFET are controlled by a single-gate electrode, just like traditional MOSFETs (15). This simplicity in control makes the TFET more compatible with existing semiconductor manufacturing processes. One of the most significant advantages of SG-

TFET is their ultra-low subthreshold leakage current. This property makes them highly energy-efficient, particularly in applications where the device spends a significant portion of its operation in standby mode and semiconductor materials play a critical role in SG-TFET performance (16, 17). Narrow bandgap materials are often preferred as they facilitate the quantum tunneling effect.SG- TFETs offer remarkable advantages in terms of subthreshold slope and power efficiency, there are challenges to overcome, such as achieving high on-state current and ensuring device reliability (18).

The Dual Material Gate Tunnel Field-Effect Transistor (DMG-TFET) is a cutting-edge semiconductor device that has gained prominence in recent years for its potential to push the boundaries of energy efficiency and performance in the field of electronics. DMG-TFETs represent an evolution of the traditional TFET by employing a unique dual-material gate structure that enhances their electrostatic analysis control over the semiconductor channel. The most distinctive feature of DMG-TFETs is their gate structure, which combines two different materials in the gate stack (19). Each material is chosen for its unique properties and compatibility with the device's operation. This dual-gate design allows for precise control of the electric field within the transistor channel (20).

The proposed device offers several potential improvements over the traditional TFET design being better control over the tunneling barrier between the source and the channel. This increased control can potentially reduce leakage currents and improve the overall performance of the transistor. The sub-threshold Swing is a key parameter indicating how efficiently a transistor can switch between on and off states. Dual gates can potentially reduce the sub-threshold swing in DG-TFETs compared to SG-TFET, leading to improved energy efficiency and it becomes possible to independently control the threshold voltages of the two gates.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS

Figure 1 shows a two dimensional cross-sectional view of proposed DMG-UOX-TFET device in 10nm. In this illustration, L1 and L2 represent the channel length and tunneling gate, respectively, while tsi, tox, and thk denote the thickness of silicon, oxide, and high-k dielectric layers in the device, respectively. The relevant device simulated parameters are presented in Table 1. This gate-engineered hetero-junction structure incorporates SiO_2 as the source material and silicon in both the channel and drain regions, thereby creating a hetero-junction within the tunneling region. Two distinct gate materials are employed with work functions, denoted as ϕ M1 and ϕ M2, set at 4.2eV and 4.8eV, respectively in the device, for the tunneling region, control region, and auxiliary region. The operation of this proposed device relies on the gate bias voltage. In the case of an n-type DMG TFET, achieving the ON state depends on increasing the positive voltage applied to the gate. This action narrows the energy barrier between the SiO_2 source and the intrinsic region. Consequently, the energy band diagram within the intrinsic region are pushed down, facilitating the tunneling of electrons from the valence band of the p-doped silicon source to the conduction band within the intrinsic SiO_2 body, a process known as band-to-band (BTB) tunneling. Subsequently, these electrons move toward the n-doped drain region through drift diffusion (21).

The structure of proposed device implemented using reduced nano dimensions has been simulated in ON and OFF state and correspondingly mesh structure, electric

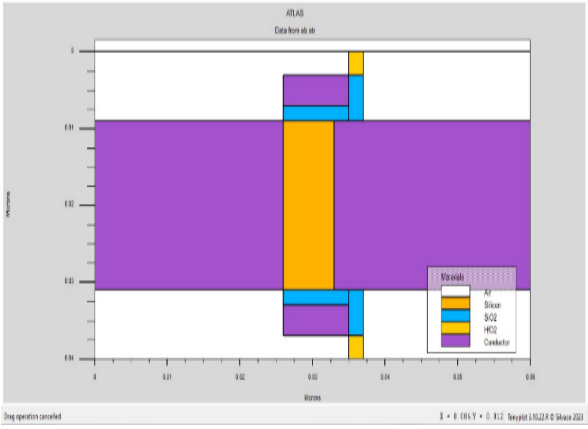

Figure 1. Proposed DMG-UOX-TFET device with differential gate oxide thickness of 1.5nm and 2nm

TABLE 1. Utilized Parameter for the simulation

Utilized Parameters	Proposed device
Thickness of SiO_2	2nm
Thickness of HfO_2	3nm
Metal Gate-1 Work Function (W_F)	4.8eV
Metal Gate-2 Work Function (W_F)	4.2eV
Device Length (W_L)	60 nm
Gate Length (L_G)	10 nm
Source Length (L_S)	25nm
Drain Length (L_D)	25nm
Channel Length (L_C)	10nm
Doping of Source (N_S)	$1x10^{20}$ cm^{-3}
Doping of Drain (N_D)	$1x10^{18}$ cm^{-3}
Doping of Channel (N_C)	$1x10^{17}$ cm^{-3}

field distribution**,** and potential distributions employed using Silvaco TCAD ATLAS tool shown in Figures 2, 3 and 4, respectively. In literature, some models have suggested using a channel length of less than 100 nm to mitigate short-channel effects in electronic devices (22). To comprehensively consider all effects in the nanoscale range, and employed the BTBT model within the ATLAS simulator due to its superior convergence properties. In this work, silicon was chosen as the source and channel material, and the gate dielectric was utilized as SiO_2 and hafnium oxide (HfO_2). The source doping level is set to Ns = $5\times10^{18}cm^{-3}$, and the drain doping level was Nd = $5\times10^{19}cm^{-3}$ and assessed the performance of the proposed device using Silvaco TCAD numerical simulator (23).

The advantages of the proposed devices are enhanced control over tunneling, improved electrostatic control, optimized threshold voltages, potential reduction in drain-induced barrier lowering, and improved current ON/OFF ratio. The disadvantages of this device are the complex fabrication process and increased design complexity.

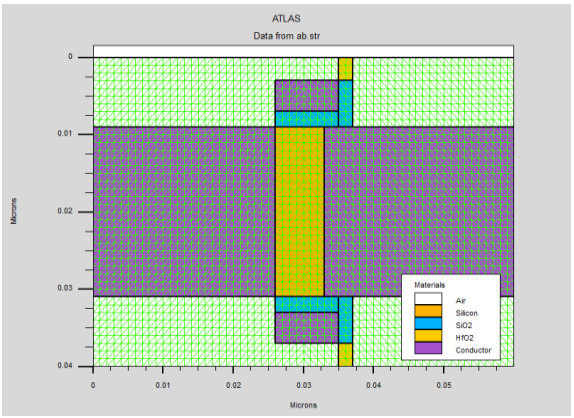

Figure 2. Mesh structure with differential gate oxide hickness of 1.5nm and 2nm

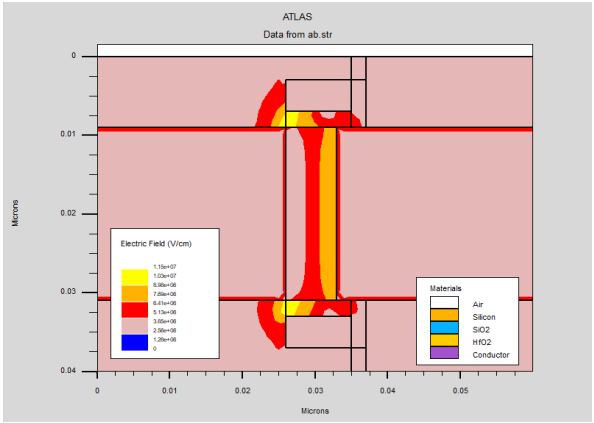

Figure 3. Electric field distribution with differential gate oxide hickness of 1.5nm and 2nm

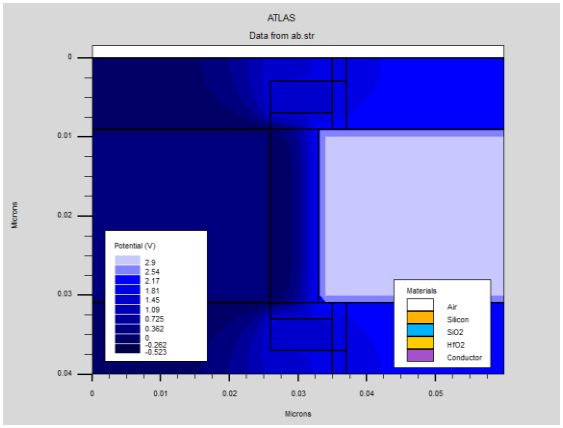

Figure 4. Potential distribution with differential gate oxide hickness of 1.5nm and 2nm

The proposed device controls the current over the two gates. This dual-gate architecture offers enhanced flexibility in tuning device characteristics and allows for precise control over the gate oxide thickness. This control can contribute to optimized tunneling band to band barrier characteristics, potentially reducing leakage currents and improving overall device performance. The DG-TFET provides improved electrostatic control over the intrinsic channel, offering the potential for reduced subthreshold swing and enhanced carrier concentration.

3. RESULTS AND DISCUSSION

3. 1. Drain current Characteristics The peak drain current for both the conventional device and the proposed structure is achieved under zero gate voltage conditions while operating in depletion mode. This is evident in the case of proposed devices in a 10nm technology, as shown in Figure 5. The graph illustrates a substantial increase in drain current as the gate oxide thickness overlaps with a constant gate voltage (VG=0) (24). In the TFET, it is imperative to deplete the upper region of the intrinsic channel through gate channel bias. Consequently, the carriers near the bottom of the channel experience a lateral movement, resulting in the flow of drain current. Consequently, the improved drain current predominantly flows in the lower region of the channel (25, 26). Consequently, the proposed device exhibits several advantages, including maximum velocity, the highest electron density, an effective channel depth, and optimal drain current flow in the channel. The drain current characteristics of the proposed dielectric material structure, maintain fixed device dimensions within a 32nm technology and a channel length (Lg) of 10nm. This configuration outperforms the conventional device, as evidenced by the simulation results. The drain current experiences a significant boost as device dimensions are minimized, along with a reduction in channel length.

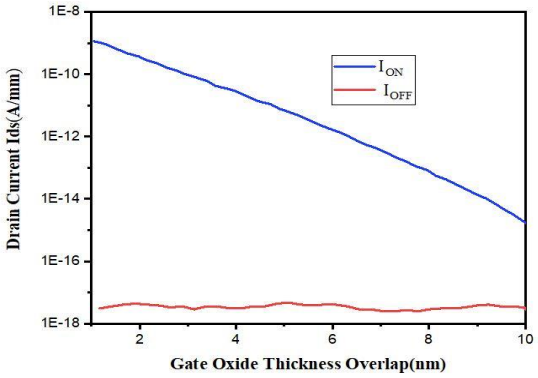

Figure 5. Drain current with gate oxide thickness overlap of the proposed device at 12 nanometer

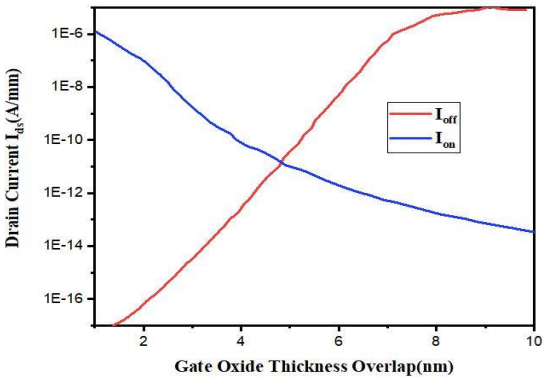

Figure 6. Drain current with gate oxide thickness overlap of the proposed device at 10 nanometer

The drain current is derived by analyzing the drain voltage while varying the gate oxide material. It is crucial to achieve an enhanced drain current. The saturated drain current (Ids) is determined by varying the gate voltage (Vgs) using different materials for the gate oxide. As the device dimensions and channel length decrease, there is a significant increase in drain current. The maximum drain current for the proposed device is attained at Vg=0.6V and Vg=2V. The increase in drain current is associated with a rise in drain voltage, facilitating the movement of electrons within the channel.

Figure 6 illustrates the relationship between Drain current and gate oxide thickness for the proposed device at a fixed Vds of 2V. When the separation between the drain and the channel is substantial, the gate primarily exercises control over channel carriers. This advanced structure exhibits the potential for enhancing drain current while maintaining a balance in the nano scale device performance (27). As depicted in the figure, an incremental increase in drain current corresponds to a decrease in off current. This behavior is attributed to the electric field crowding effect, which is more pronounced near the gate close to the drain. Consequently, there is a higher concentration of electric field compared to conventional devices. The proposed high-k structure intensifies this electric field concentration compared to the electric field distribution in Silicon Carbide (28, 29). In the drift region, the HfO_2 material necessitates a higher electric field for breakdown, resulting in the occurrence of a high electric field at elevated drain voltages (Vd). Applying a higher drain voltage in this proposed structure leads to an increased breakdown voltage within the SiO_2 structure in 10nm technology. Consequently, the electric field diminishes at the interface between the channel and the drain (30).

The on-state current and off-state current of the proposed device at various doping concentrations, gate lengths are shown in Table 2 and gate lengths of 12 nanometers and 10 nanometers node regime are tabulated and compared with conventional TFET, SG- TFET and double gates are shown in Tables 3, 4, 5 and 6.

TABLE 2. On current and off current at different doping concentrations

Doping Concentration N_D(cm^-3)	Ion (A/μm)	Ioff (A/μm)	Ion/ Ioff
1X10^18	$1.14e^{-09}$	$3.09407e^{-18}$	368332465.5
5X10^18	$1.192e^{-06}$	$4.00396e^{-18}$	$2.97749e^{+11}$
1X10^19	$1.173e^{-05}$	$1.44904e^{-12}$	8093753.993

3. 2. Drain Current with Gate Oxide Thickness

Figure 7 illustrates the drain current characteristics of the proposed structures developed in the context of 10nm technological innovations. These structures exhibit a reduced electric field concentration on the drain side. Notably, in the 10nm technology setting, the newly devised device demonstrates a higher peak electric field distribution. Consequently, an improved breakdown voltage is achieved by mitigating the electric field around the gate (G) and drain (D) regions. The simulation of the proposed TFET involves the use of three different materials. The performance analysis reveals that the HfO_2 material outperforms the other materials, yielding more favorable performance parameters. The utilization of HfO_2 material leads to an increase in drain current, indicating its superior suitability for the device. Therefore, the proposed device lies in its application for low-power applications (31).

3. 2. Drain Current Comparison at 10nm Node

Figure 8 shows the drain current (Id) as a function of gate voltage (Vg) while varying the oxide thickness (Tox) in a TFET. The proposed device dimensions and material properties, except for the oxide thickness. The oxide thicknesses range from 2 nm to 5 nm, with increments of

TABLE 3. On current and off current at Nd= 1×10^{18} cm^{-3} at gate length of 12 nano meter

Device	**Ion** (A/μm)	**Ioff** (A/μm)	**Ion/ Ioff**
C TFET	1.20529	$1.94599e^{-17}$	$1.05495e^{+13}$
SMG TFET	1.22274	$1.15327e^{-10}$	1931345.624
DMG TFET	1.1575	$6.64446e^{-12}$	23703910.57
DMG DOX TFET	0.17263	$2.59633e^{-14}$	6649056142

TABLE 4. On current and off current at Nd= 1×10^{18} cm^{-3} at gate length of 10 nano meter

Device	**Ion** (A/μm)	**Ioff** (A/μm)	**Ion/ Ioff**
C TFET	1.22271	$2.36543e^{-16}$	$9.41521e^{11}$
SMG TFET	1.174301	$2.42382e^{-11}$	7191177.358
DMG TFET	1.204597	$3.69445e^{-10}$	553796.2365
DMG DOX TFET	1.148494	$1.68717e^{-13}$	880136435.3

TABLE 5. On current and off current at Nd= 5×10^{18} cm^{-3} at gate length of 12 nano meter

Device	**Ion** (A/μm)	**Ioff** (A/μm)	**Ion/ Ioff**
C TFET	1.114425	$7.12968e^{-12}$	16049074.76
SMG TFET	1.106412	$8.31917e^{-12}$	12791162.02
DMG TFET	1.114425	$3.98511e^{-09}$	28713.09448
DMG DOX TFET	$9.80641e^{-05}$	$2.79177e^{-13}$	351261053.9

TABLE 6. On current and off current at Nd= 5×10^{18} cm^{-3} at gate length of 10 nano meter

Device	**Ion** (A/μm)	**Ioff** (A/μm)	**Ion/ Ioff**
C TFET	1.355803	$2.93691e^{-08}$	12114.90464
SMG TFET	1.505557	$1.59643e^{-08}$	31667.9536
DMG TFET	1.10405	$5.92953e^{-08}$	1754.769188
DMG DOX TFET	1.250409	$8.75488e^{-10}$	286022.3694

1 nm. The TFET with a thinner oxide exhibited a lower sub-threshold voltage (Vth), which implies that it can turn on at lower gate voltage. The drain current increased more rapidly with gate voltage for TFETs with thinner oxides, indicating improved on-current performance (32). The sub-threshold slope, representing the steepness of the Id-Vg curve, was smaller for thinner oxide TFETs for better-switching characteristics. In a single-gate TFET, increasing the gate voltage typically increases the drain current, as it controls the tunneling of electrons or holes through the tunnel junction. However, this effect is usually nonlinear due to the unique band structure of TFETs shown in Figure 9. The oxide thickness can influence the TFET's performance by affecting the tunneling probability and the sub-threshold slope. A

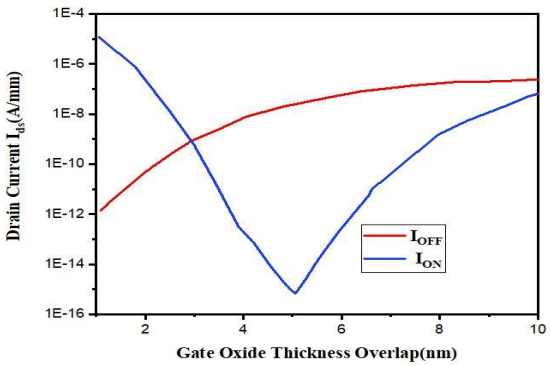

Figure 7. Drain current with gate oxide thickness overlap of the proposed device with Nd= 5×10^{18} cm^{-3} at gate length of 10 nanometer

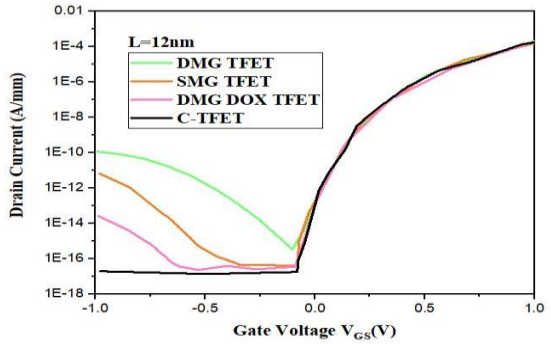

Figure 8. Drain current with gate voltage of various structures at 12 nanometer node

thinner oxide layer generally results in better tunneling and lower sub-threshold slope, leading to higher drain currents. In dual gate TFETs, there are two gate voltages Vg1 and Vg2. Vg1 controls the tunneling barrier and impacts the drain current similarly to a SG-TFET. Vg2 often called the modulation gate, allows for additional control over the tunneling and can further enhance the drain current. A thinner oxide layer still tends to improve performance, but the dual gate TFET will provide more opportunities for control and optimization. Oxide thickness indirectly affects the TFET performance by influencing the gate voltage needed to achieve a certain drain current. Thinner oxide layers generally require lower gate voltages to control tunneling effectively. Lower oxide thickness tends to result in better TFET performance, with lower sub-threshold slopes and higher drain currents as shown in Figure 10.

The proposed device exhibits a drain conductance related to 6H-SiC and SiO_2 dielectric materials. This superiority in drain conductance contributes to the device achieving the highest packing density, attributed to the enhanced current flow within the device. Consequently, this structural advantage of the proposed device results in a notable improvement and improved characteristics of

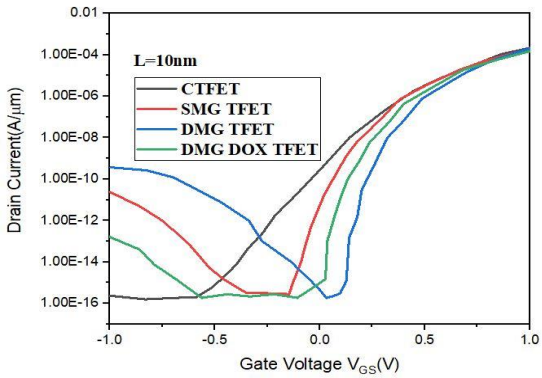

Figure 9. Drain current with gate voltage of various structures at 10 nanometer node

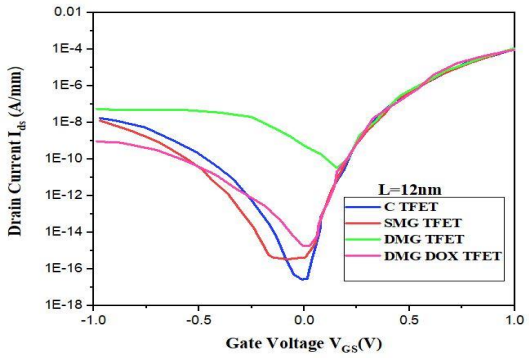

Figure 10. Drain current with gate voltage of various structures at 12 nanometer node at a different doping concentration

transconductance. A high transconductance is imperative for achieving proper device gain. However, the reduction in subthreshold slope, while desirable, leads to increased off-current and power dissipation within the device.

4. CONCLUSION

The performance analysis of DMG-UOX-TFET with variation of oxide materials is analysed using TCAD ATLAS simulator in 10nm node . This device features a hetero-junction formed by combining silicon materials and hafnium oxide in the drain-channel junction. Additionally, it utilizes a hetero-dielectric gate stack comprising SiO_2 and HfO_2 where HfO_2 holds substantial promise as a semiconductor material for high-voltage and high-frequency applications, including cosmic cells and energy devices. The proposed structure, designed for 10nm innovations and employing Silvaco TCAD, exhibits notable enhancements in electrical properties such as On current (Ion), Off current (Ioff), Ion/Ioff ratio, as well as RF properties like drain conductance (Gd) and On resistance (Ron). Therefore, this proposed structure is well suited for low-power applications.

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Persian Abstract

چکیده

مدل‌سازی تحلیلی دو بعدی ترانزیستور اثر میدانی تونل دروازه دوگانه با تغییر در تغییر ضخامت اکسید گیت (DMG-UOX-TFET) در این کار پیشنهاد شده‌است. این دستگاه پیشنهادی از مواد دی الکتریک مانند اکسید هافنیوم و دی اکسید سیلیکون با ضخامت های اکسید متمایز استفاده می کند. این دستگاه با استفاده از یک ابزار طراحی کامپیوتری به کمک فناوری در فناوری ۱۰ نانومتر (۰.۰۱ میکرومتر) اختراع شد. این کار تاثیر ضخامت اکسید گیت را بر ویژگی‌های الکتریکی دستگاه پیشنهادی، با تمرکز ویژه بر تغییرات جریان تخلیه بررسی می‌کند. شبیه‌سازی‌های گسترده و پارامترهای عملکرد کلیدی دستگاه پیشنهادی با توجه به ضخامت اکسید گیت تحلیل می‌شوند. ضخامت‌های مختلف اکسید گیت و تأثیرات آن‌ها بر شیب آستانه فرعی دستگاه، نسبت جریان روشن، جریان خاموش و نسبت جریان خاموش، تحلیل می‌شوند. دستگاه پیشنهادی عملیات‌های نوع n را در ناحیه همپوشانی دروازه ترکیب می‌کند، که به طور موثر اثر گوشه و تونل‌زنی مضر نوار به باند را کاهش می‌دهد که می‌تواند نسبت روشن/خاموش را کاهش دهد. از طریق بهینه‌سازی دقیق غلظت دوپینگ در ناحیه همپوشانی دروازه، به افزایش قابل‌توجه ٤.٨ زمان در جریان پیوسته دست یافت، در حالی که به طور همزمان میانگین نوسان زیرآستانه را از ۹۱.۳ mV/dec به ۵۲.۸ mV/dec کاهش داد.