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Design and Simulation of a Novel Hetero-junction Bipolar Transistor with Gate-Controlled Current Gain

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ABSTRACT

A new structure for SiGe Hetero-junction Bipolar transistor (HBT) is designed and simulated using Silvaco simulator. The considered extra terminal gives the ability to control the transistor's current gain. By applying voltage to the gate terminal, the base effective width would be controlled. Decrement of the Base width yields to the carrier recombination rate reduction, let the emitted electrons to have higher chance to reach the collector. Considering extra terminal have two approaches. One is to improve the current gain of the transistor by applying a constant voltage to the gate and the other is to modify the characteristics of the transistor in such a way that the current gain became optimized. The current gain of the transistor without any gate voltage is about 50V, which increases to 750 for high and 50,000 for low collector currents with the gate voltage variation consideration. In addition, our final proposed gate-controlled HBT with a large gate over the base and collector has the breakdown voltage of 8V and the cut-off frequency of about 11 GHz. The maximum FoM of 1200 is achieved using the proposed structure.

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1. INTRODUCTION

In semiconductor technology, both bipolar and field effect transistors are required for various analog and digital applications. In fact, these two technologies are complementary. Bipolar Complementary Metal-Oxide Semiconductor (BiCMOS) technology uses both types of transistors to take their advantages to build more complex and convenient circuits [1, 2]. Although there are many innovations in the design and fabrication of new transistor structures such as carbon nanotube field effect transistors (CNTFET) [2, 3] and QCA structures [4]. It is predicted that the electronics industry will move towards the use of these devices, but there is still a need to use bipolar transistors in a lot of high power or high frequency applications [5]. In Radio Frequency (RF) applications, BJTs are superior to field effect ones [6], but in terms of the number of in-chip transistors, MOSFET transistors are superior. In BJTs, the current gain (β) is one of the most important parameters [7], which is determined during the design and fabrication processes and the manufacturing technology, which may change with factors such as temperature and affect the circuit operation. There is also a great desire to increase or control this parameter using different techniques [8].

Considering the suggestion to add another terminal to BJTs, which is called gate; it is possible to change the current gain of a bipolar transistor. The above device is made in two conventional CMOS technologies [9]. To increase the gain of bipolar transistors, heterogeneous junction is used in Base-Emitter contact [10]. As the integration of two types of transistors on a chip is challenging [11], bipolar transistors based on SOI have been studied and built because of the fact that they are used in system-on-chip (SoC) structures [12-15]. According to the applied bias voltage, it is possible to increase the gain of the transistor by the application a constant voltage to the gate terminal [16]. Due to the application of Heterojunction Bipolar Transistor (HBT) structure, the final proposed structure is expected to have higher speed and efficiency compared to the conventional bipolar junction transistors (BJTs) [17].

A hybrid-mode device based on a standard sub-micrometer CMOS technology is presented as a

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MOSFET in which the gate and the well are internally connected to form the base of a lateral BJT. At low collector current levels, lateral bipolar action with a current gain higher than 1000 is achieved [18]. Moreover, a CMOS-compatible gate-controlled lateral BJT (GC-LBJT) is fabricated with a conventional 90 nm CMOS technology for RF applications. The Emitter injection efficiency and the doping profile of P-well were optimized by properly controlling source, drain, and well implants. Consequently, the GC-LBJT with the Gate length of 0.15μm would achieve a current gain over than 2000 and f_T/f_{max} ratio of about 17/19, which compare to previously reported LBJT, yield to the improvements of 1000%, 200%, and 60% in current gain, f_T and f_{max}, respectively [19].

Bipolar devices are widely used in the nuclear reactor control systems, and the radiation effects are challenging in their operation. The lateral PNP BJT is a radiation-sensitive structure in bipolar integrated devices. Its degradation under irradiation is the primary cause for functional failures of these devices. It is useful to estimate the radiation response of the transistors to find better design strategies for radiation hardness. Three kinds of gate-controlled lateral PNP transistors (GCL-PNPs) with different base widths and doping concentrations are specially designed to explore base current degradation induced by reactor neutrons and gamma rays. Dependence on base width and doping concentration of the degradation is analyzed in this work and the results are beneficial to radiation-hardening design of the lateral PNP BJT [20].

2. NEW DEVICE STRUCTURE

Controlling the current gain of a bipolar structure using the gate terminal has been discussed for BJTs and not for a HBT structure in previous investigations. This work studies the effect of adding the gate terminal to a SiGe HBT which has not been previously discussed. Figure 1 shows the structure of a 1-um width HBT transistor with a base made of SiGe in Silvaco software. To implement this structure, the Atlas environment of Silvaco software has been used. This novel structure is a bipolar transistor which has four terminals. In the upper part of the transistor, like MOSFETs, there is a SiO_2 insulation layer between the gate and substrate. The length of the transistor is considered as 2 microns and physical width of the base is 300 nanometers. Furthermore, the oxide thickness is equal to 100 nm and the space of 50 nm is provided between the terminals of the transistor to prevent them from affecting each other. In addition, the gate plate, which is placed on the oxide, covers about half of the base and part of the collector. The collector, base and emitter widths are 0.85, 0.3 and 0.85 microns, respectively.

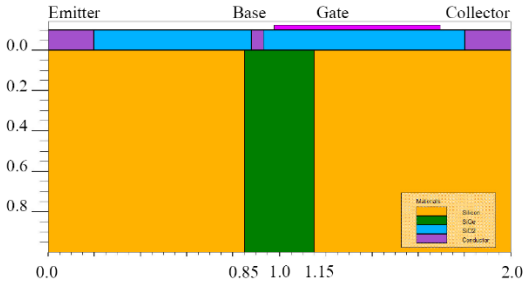

Figure 1. Structure of the proposed HBT transistor

The doping distribution of different regions of the transistor is shown in Figure 2. This transistor is an n-p-n type and the doping of the collector, base and emitter regions are 1×10^{15}, 3×10^{16} and 5×10^{18} cm^{-3}, respectively. Compare to a BJT, it is possible to increase the base doping to have a higher f_T, without any degradation in current gain value. To have ohmic contacts, n^+ and p^+ regions are used beneath the surface to make connection with the collector and the base metals.

3. SILVACO SIMULATIONS

In this article, all the simulations have been performed using Silvaco device simulator in order to investigate the electrical behavior of the proposed structure. The sizes and doping levels of the structure are optimized to reach the optimum performance point.

The gate contact in the proposed structure controls the base width, through which the transistor current gain will be controlled. When the Gate voltage is zero, there are no changes in the base width and the transistor current gain totally depends on doping values, thicknesses and dimensions. On the other hand, by applying a positive voltage on the gate contact, an inversion region would be formed under the gate. As a result, a portion of the p-base region will be converted to an n-region, merges to the collector part. In the proposed transistor, the gate length is designed to cover half of the base width. It is important to note that there is not any MOS structure in the proposed transistor design because the gate covers a part of the p-base region.

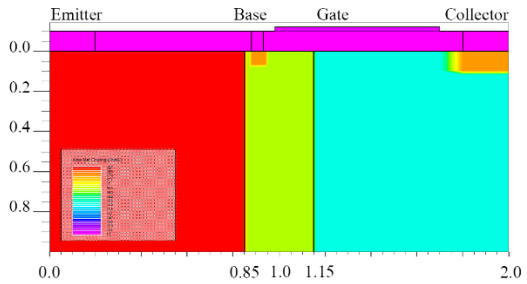

Figure 2. Doping distribution of the structure in Silvaco

As the gate position and its length have a major effect on the transistor characterization, we have considered them as two variable parameters in our simulations. By increasing the gate length, its capacitance with the substrate increases which yield to the absorption of carriers transporting from base to the collector to the SiO_2 layer beneath and forming a path with lower resistance for the passing carriers. This point tends to a lower base resistance, higher cut-off frequency and much more current gain. The gate length increases up to the point where it affects the functionality of the base and collector contacts.

3. 1. Gate Position In this simulation, to find the appropriate location of the gate and its optimized size, the device is simulated without gate and the currents of base and collector are measured. The profile of current density of the device due to the application of 3V collector voltage and 650mV base voltage is shown in Figure 3. In this case, the current path is at all depths of the device and the electrons path is determined by the collector and emitter terminals voltages and the non-uniform internal electrical field of the collector-emitter junction.

Figure 4 demonstrates the base and collector currents in terms of the base-emitter voltage while the emitter is grounded. According to this curves, it is obvious that the collector current is a coefficient of the base current and by dividing the collector current to the base one at each point, the value of β would be calculated. The obtained β for this transistor is 50, which is acceptable and the structure can be used to investigate the effect of adding gate to the device.

To add the gate terminal to this structure, a layer of silicon oxide is considered. Figures 5 to 8 implies the current density profiles for four different modes of gate location and size. Also, Table 1 summarized the device specifications in these modes. Considering the obtained results, the multiplication of β and break down voltage as the figure of merit (FoM) of the structure, increases about 70% using gate in our structure. Moreover, using a large gate on collector yields to an improvement of about 175% and 200% for the cut-off frequency and β values,

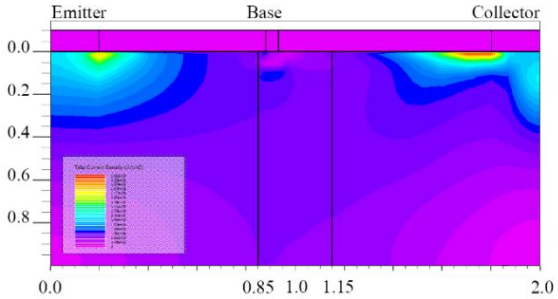

Figure 3. Device currents density without considering the Gate voltage

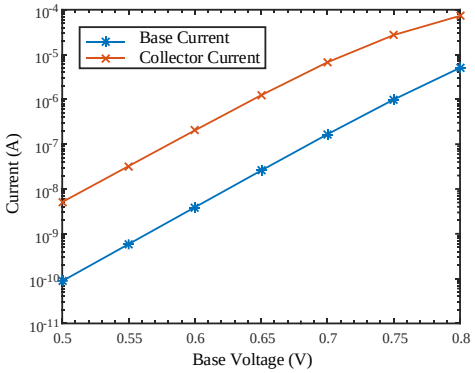

Figure 4. Base and Collector currents without applying the Gate voltage

respectively; while the break down voltage at the worst case has the degradation of about 38%. As the large gate condition has the most FoM and f_T values, it is selected as the final proposed structure.

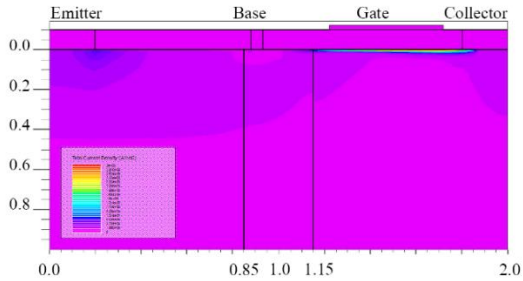

Figure 5. Device current density with gate on collector

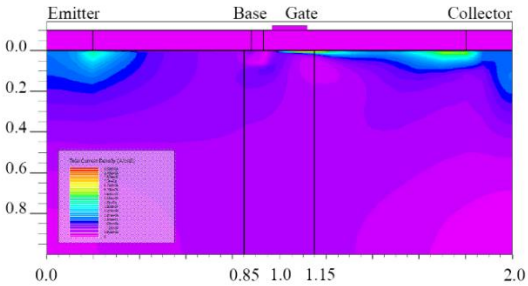

Figure 6. Device current density with gate on base

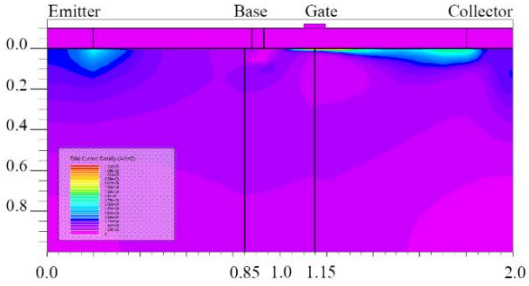

Figure 7. Device current density with small Gate

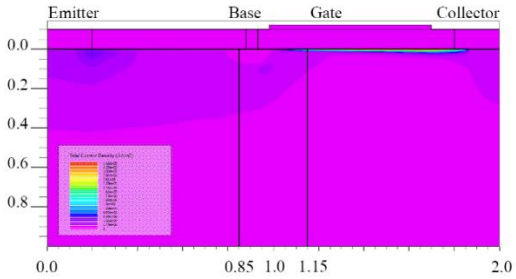

Figure 8. Device current density with large Gate

TABLE 1. Device characteristics in different modes for Gate dimensions and location

Parameter	Without Gate	Gate on Collector	Gate on Base	Small Gate	Large Gate
Collector current (μA)	1	2	1.5	1.5	3
Base current (μA)	0.02	0.02	0.02	0.02	0.02
Current gain (β)	50	100	75	75	150
Break down voltage (V_A)	13	11	10	10	8
Cut-off frequency (GHz)	4	7.6	6.7	7.1	11
FoM	650	1100	750	750	1200

Figure 9 shows the β values for all 5 different modes of gate location and size. As is apparent, with increment in base voltage, all the gain curves decreases. As the base voltage increases, the collector current tends to be saturated and the I_C/I_B ratio decreases. Among the modes, the large gate one has the most values of current gain as the inversion layer formation caused by voltage application to the gate forms a path for the carriers to reach the collector with the minimum resistivity.

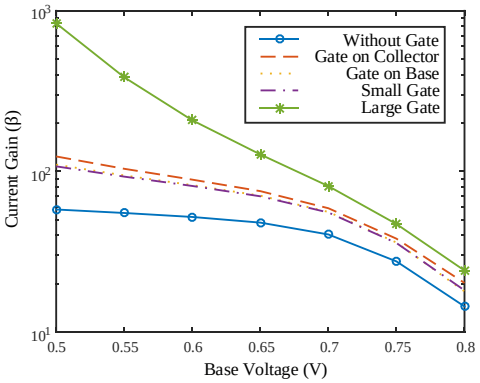

Figure 9. Variation of β versus base voltage for different gate modes

3. 2. Oxide Capacitance Another way to increase the efficiency of the gate functionality in our proposed device is to enhance the gate-oxide capacitance, which is similar to the MOS one in a field effect transistor. Considering the relation of $C_{ox} = \varepsilon \frac{A}{d}$, there are generally three methods to increase the oxide capacitance. Enlarging the surface of oxide area, reducing its thickness or substituting the oxide with a higher permittivity one. Figure 10 demonstrates the β values as a function of the base voltage for all three modes of without gate, with a 3V biased gate and oxide relative permittivity of 3.9 and 15.

Another important and effective factor is the thickness of the insulator under the gate plate. Figure 11 shows the current gain of the transistor as a function of gate voltage for different thicknesses of SiO_2. As the thickness increases, formation of the inversion layer needs a higher voltage, tends to the decrement of collector current and as a result the current gain degradation. Consequently, the thickness of 50 nm is selected for the gate oxide in our analysis and simulations.

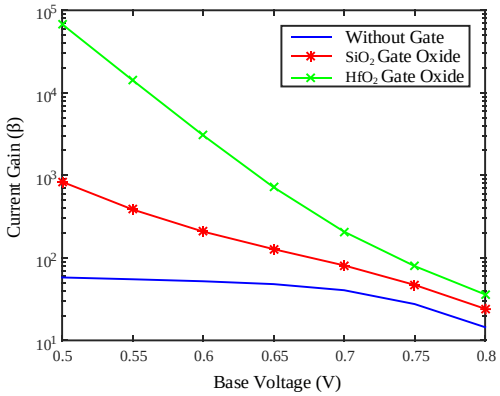

Figure 10. Values of β as a function of the base voltage

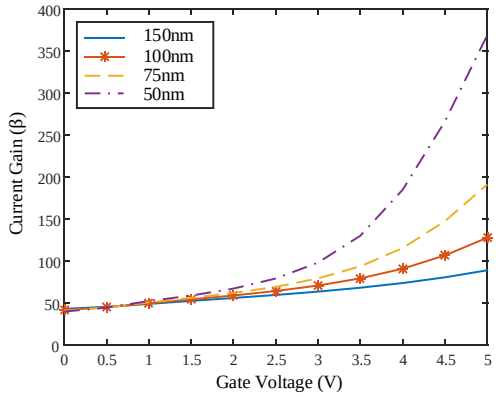

Figure 11. Current gain varations as a function of the gate voltage for different oxide thicknesses

Considering these methods for improving the device performance, the value of β is improved about 15 times more for large collector currents and even much higher than the mentioned value for low collector currents. Finally, the value of β measured at 650 mV of base voltage is increased from 50 to 750, which by changing the gate voltage from 0 to 5V, the desired gain within this range is achievable.

4. TRANSISTOR OPERATION ANALYSIS

In comparison with Si BJTs, HBTs show better performance in terms of emitter injection efficiency, base resistance, base-emitter capacitance, and cutoff frequency. They also offer good linearity, low phase noise and high power efficiency. In the proposed structure, high injection efficiency is obtained by using SiGe material with a smaller energy band gap for the base than Si, which is used as the emitter material. The large energy band-gap of emitter blocks injection of holes from the base. Therefore, the doping concentration in the base and emitter can be adjusted over a wide range with a little effect on injection efficiency, tends to higher current gain values in comparison with BJTs, without degrading the early voltage (V_A) value.

In the HBT conventional structure, due to the uniform distribution of impurities, the electric field is also uniform in space charge region. Figure 12 shows this uniform field at the base and collector junctions. The green area is the base which is made of SiGe and the yellow area on the right corresponds to the collector.

Similar to the previous figure, the electric field distribution at the base-emitter junction by the application of 5V to the considered gate is depicted in Figure 13. Here, due to the application of positive voltage to the gate and the accumulation of electrons under the oxide, a vertical field is created from top to bottom. The field intensity depends on the capacitor value and the applied voltage to the gate. Finally, by the interaction of these two fields, one with the direction from top to bottom and the other from the collector to the base, a non-uniform field would be created. The direction of this field

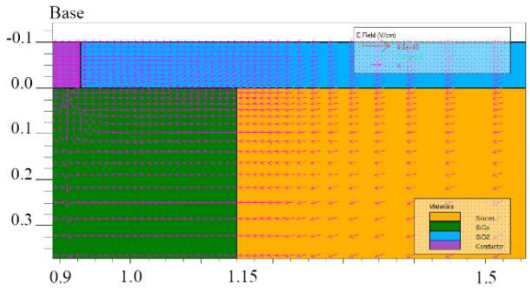

Figure 12. Direction of electric field distribution at the junction of Base and Collector

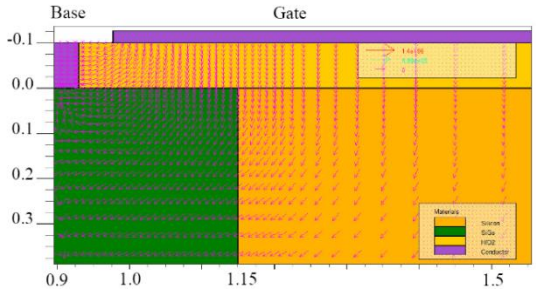

Figure 13. Non-uniform field distribusion at the junction of Base and Collector after the positive voltage application to the Gate

is from the collector to the base in the lower parts of the device and from the top to the bottom and inclined towards the base in the upper regions. This causes the electrons in the base to be attracted to the collector.

As the positive voltage is applied to the gate, electrons in the base region, similar to a MOSFET, accumulate below the gate oxide and create an inversion layer. As a result, the effective width of the base reduces just after applying the positive voltage to the gate and therefore, the current gain would increase. Moreover, Figure 14 implies the value of β as a function of the gate voltage, where the transistor is in the active region and the base voltage is 600mV.

4. 1. Breakdown Voltage Figure 15 shows the current-voltage characteristic of the transistor as a voltage of 5V is applied to the gate terminal. To find the breakdown voltage of the collector-base junction, the collector voltage is swiped from 0 to 10V for a constant current of 1nA at the base terminal. This increment in voltage should be continued until an abrupt change in the collector current occurs at the collector voltage of 8V.

4. 2. Cut-off Frequency In a bipolar transistor, the cut-off frequency is mostly related to the base width and its doping level; so the smaller the base width, the higher the cut-off frequency of the transistor. As in a bipolar

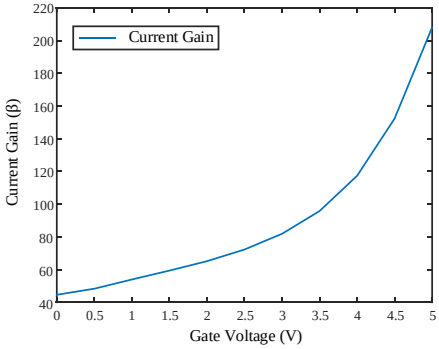

Figure 14. Values of β versus the gate voltage

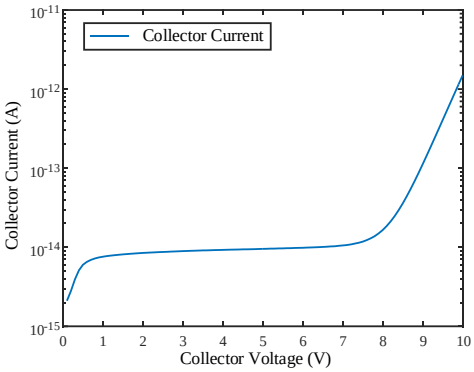

Figure 15. Collector-Base reverse breakdown voltage determination

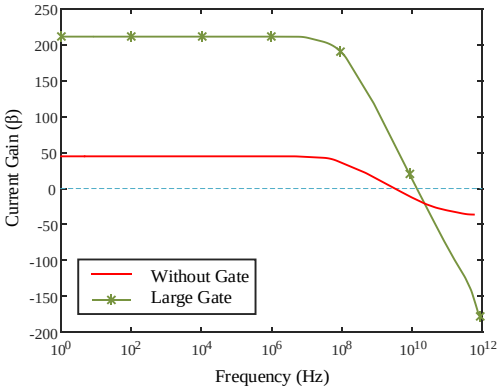

Figure 17. Values of β versuss frequency before and after consideration of the gate in the structure

transistor, the cut-off frequency is inversely related to the passage time of the carriers from the emitter to the collector. In addition, short base width yields to its smaller resistance which tends to a faster transistor operation.

Figure 16 shows the electrons accumulation under the gate plate in the base region due to the application of positive voltage to the gate. Here, a voltage of 5 volts is applied to the gate, and due to the accumulation of carriers, the electrons injected from the emitter go through the path under gate to reach the collector.

Considering no voltage application to the gate, the base width is the same as the actual value, which is defined according to the dimensions of the device. Considering this point in Figure 17, the 4 GHz cut-off frequency would be increased to 11 GHz after applying 5 volts to the gate terminal. Therefore, considering a large gate for the structure would improve not only the current gain but also the cut-off frequency.

Table 2 represents the comparison between different reports on the gain controlling of bipolar transistors. It should be noted that the β value for high currents is 750. Because in most articles, the value of β is reported for low collector currents, here the values of β, which corresponds to the base current of five μA at the base voltage of 500 mV, has been reported. Considering the product of current gain and break down voltage as the FoM of each transistor, our structure has the most value.

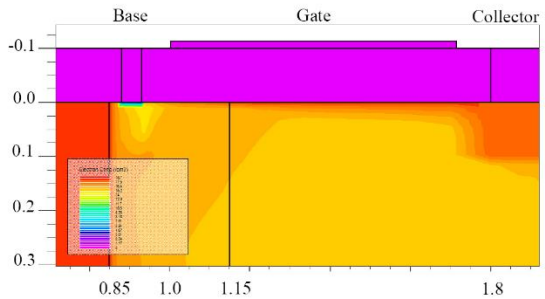

Figure 16. The electrons concentration in the structure due to the application of positive voltage to the gate

TABLE 2. Comparison table of the results with previous articles

Reference	Structure	Current gain (β)	Cut-off frequency (GHz)	Break down voltage (V)
[14]	Lateral bipolar	30	20	8.2
[19]	Combined with MOS	250	13	45.2
[7]	Combined with MOS	10000	0.1	-
[21]	Lateral bipolar	1600	13	5
[8]	Controlling the Base width	2000	25	5.7
[22]	Strained Si/SiGe HBT	2900	500	-
[23]	InP based HBT	126	5.4	-
This research (Large Gate)	Gate-controlled gain	50000	11	8

5. CONCLUSION

In this research, a new HBT structure with Gate-controlled gain is proposed and simulated by Silvaco software. The simulations were performed with SiGe Base on both conventional bipolar and Gate-controlled structures. In addition, the effect of the gate position and length on its performance are investigated and the appropriate location and dimension were determined. The simulations imply that the current gain of the transistor is acceptable, as for the gate voltage of zero, the gain of the transistor is about 50 and with the gate voltage increment to 5V, it reaches to 750 for high and even up to 50,000 for low collector currents. This

transistor also has a reasonable breakdown voltage and cut-off frequency which are about 8V and 11GHz, respectively, as the voltage is applied to the gate.

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Persian Abstract

چکیده

ساختار جدیدی برای ترانزیستور دوقطبی اتصال هترو (HBT) مبتنی بر SiGe با استفاده از شبیه‌ساز Silvaco طراحی و شبیه سازی شده است. پایه اضافی در نظر گرفته شده برای این ساختار قابلیت کنترل بهره جریان ترانزیستور را بدست می‌دهد که در نتیجه آن با اعمال ولتاژ به ترمینال گیت، عرض موثر بیس کنترل می‌شود. کاهش عرض بیس منجر به کاهش نرخ بازترکیب حامل‌ها شده و به الکترون‌های پخش شده اجازه می‌دهد شانس بیشتری برای رسیدن به کلکتور داشته باشند. لحاظ کردن پایه اضافی دو رویکرد را در نظر دارد. یکی بهبود بهره جریان ترانزیستور با اعمال ولتاژ ثابت به گیت و دیگری اصلاح ویژگی‌های ترانزیستور بگونه‌ای که بهره جریان بهینه شود. بهره جریان ترانزیستور بدون اعمال ولتاژ گیت حدود ۵۰ است که با در نظر گرفتن تغییرات ولتاژ گیت تا ۷۵۰ برای جریان های کلکتور زیاد و ۵۰۰۰۰ برای جریان های کلکتور کم، افزایش می‌یابد. علاوه بر این، ساختار HBT کنترل شده با گیت پیشنهادی ما با یک گیت بزرگ روی بیس و کلکتور دارای ولتاژ شکست ۸ ولت و فرکانس قطع حدود ۱۱ گیگاهرتز است. همچنین حداکثر ضریب شایستگی ۱۲۰۰ با استفاده از ساختار پیشنهادی به دست می‌آید.