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A 65 nm CMOS Feedforward Transimpedance Amplifier for Optical Fibers Communications

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ABSTRACT

A series of inductor loads may not be the best design criterion for improvement in circuit performance. In this work, the best compromise so far for the trade-off in power consumption, input referred noise current spectral density, with wide bandwidth, high transimpedance gain and low DC supply voltage is reported. A simulated 65 nm CMOS feedforward transimpedance amplifier is introduced with a series of single PMOS loads instead of a series of inductor loads. A bandwidth of 20.16 GHz with a transimpedance gain of 51.16 dBΩ, an input referred noise current spectral density of 34.3 p A/√Hz, a power consumption of 1.052 mW and with a 1V DC supply voltage are presented. In addition, an active inductor load (instead of inductor load) is introduced within the 65 nm CMOS feedforward transimpedance amplifier. A bandwidth of 3.75 GHz with a transimpedance gain of 42.7 dBΩ, an input referred noise current spectral density of 21.4 p A/√Hz, a power consumption of 0.66 mW and with a 1V DC supply voltage are reported. This 65 nm CMOS feedforward design process provides enough voltage headrom for gate-to-source terminals in amplifying transistors due to less DC voltage drop across PMOS loads. As a result, this design process consumes the lowest possible power consumption especially with the single PMOS loads as well as with the active inductor load.

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1. INTRODUCTION

Demands have risen for Giga bit per second fiber optic receivers due to ever growing data transmission in various communication systems. Front-end optical preamplifiers in the form of transimpedance amplifers (TIA) have become a viable optical receiver option as a first stage integrated within a comprehensive optical communication system. The search for low-power transimpedance amplifiers with wide bandwidth lead to the common form of regulated cascode (RGC) used in optical receiver topologies [1-6]. However, modification of the RGC structure in terms of input impedance has been the subject for research to achieve wider bandwidths. Structures such as T-matching network [1], series inductor peaking [2], a capacitive degeneration technique [4], a common-gate feedforward TIA [7], a dual-mode feedforward TIA [8] and a feedforward current amplifier TIA [9] were considered. In terms of 65 nm CMOS process technology, various topologies were reported such as an modified RGC TIA using peaking inductors [10], an RGC block and a differential amplifier with active feedback TIA [11] and adjustable gain peaking TIA [12]. In terms of modulated-wavelength division radio signals over an optical fiber, hybrid optical sources were used for better performance of a fiber communication network [13]. Advanced technologies work in conjunction with fiber networks include Internet of Things (IOT) based 5G networks in which an algorithm based on physical key layer generation (PLKG) and Physical Layer Encryption were used as measures for protection [14]. Wideband inductive elements were utilized in order to design I/O impedance matching circuits given the capacitive nature of I/O impedances of millimeter wave amplifiers [15]. Millimeter wave low noise amplifiers were utilized in 65 nm common-gate inductive feedback by adopting a gate inductor within a cascode stage [16].

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1. 1. Common-Gate Feedforward Transimpedance Amplifier In Figure 1a, transistor M_2 operates as a common gate stage and also being in a feedback loop, it works as a source follower. Resistor R_2 is equivalent to the overall TIA gain at low frequencies. If the loop at M_2 gate is broken, provided that body effect and channel length modulation are neglected, the input resistance is represented by Razavi [17]:

$$R_{in} = \frac{1}{g_{m2}}\left(\frac{1}{1+g_{m1}R_1}\right) \quad (1)$$

Due to the feedback loop, the input resistance is lowered, hence, the bandwidth is extended. The circuit in Figure 1a can be redrawn as in Figure 1b which is basically a feedforward amplifier that drives the gate of transistor M_2 which is in a common source formation. Theoretically, an ideal current source I_B leads to make resistor R_2 as the only major noise contributor since there is no noise current that emerges from the drain of transistor M_2. In practice, the input referred current noise is as follows [17]:

$$\overline{I_{in}^2} = \frac{4kT}{R_2} + \overline{I_{n,B}^2} \quad (2)$$

Equation (2) is similar to the input referred noise current for the common gate stage which proves that the feedforward case does not contribute to the noise rise while it lowers input resistance.

One drawback arises from Figure 1a in which the bias voltage at node X approaches $V_{gs1} + V_{gs2}$ which imposes a voltage drop limitation across resistor R_1 and hence lowering gain $g_{m1}R_1$. However, an alternative is available which is in the addition of level shifter to the circuit in Figure 1(b) with an inclusion of a common gate as in Figure 2. The amount of voltage at node X can now be available to overcome V_{gs2} (only) and hence enables the current path for I_B. The input resistance can be summarized as follows [17]:

$$R_{in} = \frac{1}{g_{m3}+(1+g_{m3}R_3g_{m1}R_1)g_{m2}} \quad (3)$$

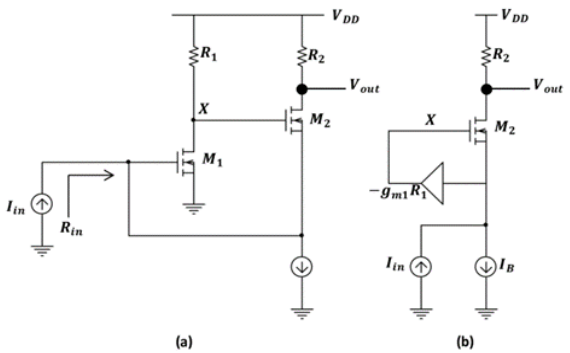

Figure 1. (a) TIA in feedback form, (b) Amplifier inserted in feedforward path [17]

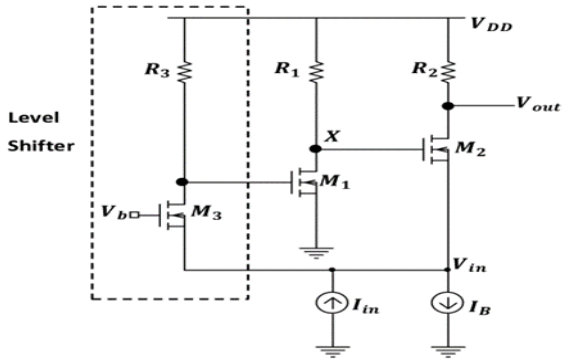

Figure 2. Feedforward path in TIA [12]

It is obvious from Equation (3) that the input resistance is lowered (by a factor of $1 + g_{m3}R_3g_{m1}R_1$).

The output resistance of the circuit in Figure 2 is stated below [17].

$$R_o = \frac{g_{m2}R_2(1+g_{m3}R_3g_{m1}R_1)}{g_{m3}+(1+g_{m3}R_3g_{m1}R_1)g_{m2}} \quad (4)$$

The output resistance R_o is nearly equal to R_2 given that $(1 + g_{m3}R_3g_{m1}R_1)g_{m2} \gg g_{m3}$. It shows that this circuit does have a transimpedance gain of a common gate stage, however, with a significant reduction of the input resistance.

1. 2. Main Contribution of this Work The main contribution of this work is to provide tangible evidence that Single PMOS Loads (SPL) TIA is a better alternative than inductor loads TIA in terms of circuit performance. In addition, to illustrate that an Active Inductor Load (AIL) TIA can have a much lower power consumption and input referred noise current in comparison with inductor loads TIA. The SPL TIA and the AIL TIA are aimed for 20 Gb/s and 3.5 Gb/s applications, respectively.

2. PROPOSED TIA TOPOLOGIES

2. 1. SPL TIA The proposed 65 nm CMOS Common-Gate feedforward SPL TIA configuration is shown in Figure 3 which is a development of a previous work [9]. In this work, no inductor based current sources were used and instead, low aspect ratio (W/L) PMOS transistors (M_5, M_6 and M_7) were connected. Down to 65 nm imposes short channel effects in which MOSFETs drain current roughly becomes [18]:

$$I_D = \frac{1}{2}\left(\frac{\mu_0 C_{ox}}{1+\theta(V_{gs}-V_{th})}\right)\frac{W}{L}\left(V_{gs}-V_{th}\right)^2 \quad (5)$$

where θ is the fitting parameter that is roughly equals to $(10^{-7}/t_{ox})$ V^{-1}. A 65 nm Predictive Technology Model (PTM) is utilized throughout LTspice XVII simulation

run of the envisaged TIA design. The presence of NMOS transistor M_2 (DC level shifting of NMOS transistor M_3) makes it easier to accommodate V_{gs3} and therefore enabling wider headroom for faster sinking of M_3 drain current. Serving as an amplifier in a local feedback form, NMOS transistor M_1 showed a finite voltage amplification from node Y to node O. The (W/L) aspect ratio for the PMOS and NMOS transistors used in this work is as follows:

The aspect ratios shown in Table 1 proved to be optimal for 1V DC supply voltage that contributed to the lowest noise and power consumption reported in this work for 65 nm CMOS process. However, these ratios can be applied for other processes, though, noise and power consumption can be a challenge. Compatibility with 65 nm CMOS process required 100 fF photodiode capacitance (C_{PD}) in which the total input capacitance is $C_{in,tot} = C_{PD} + C_{db4} + C_{sb1} + C_{sb2}$, while the load capacitance C_L was in the order of 200 fF. The node Y (the drain of transistor M_3) can now easily accommodate the gate-to-source voltage of transistor M_1 given the fact that DC voltage-level raising capability of transistor M_2 has the input source of transistor M_1 from the gate of transistor M_3. From another standpoint, low voltage drop on PMOS loads serves the same purpose.

The design process in Figure 3 overcomes many problems associated with classic regulated cascode (RGC) which has no M2 transistor presence. RGC drawbacks include the need to have two gate-to-source voltages at node Y and that may exceed the 1V budget supply. In addition, in RGC topology, there has to be enough voltage room at the output node for drain-to-source saturation with an additional gate-to-source voltage. The presence of M2 transistor in feedforward design enables biasing of transistors M1 and M3 at half of the budget DC voltage value. This design concept along with the discussion stated in section 4.1 relating to the advantages of SPL versus classic inductor loads clarify the reasons behind the selection of the design shown in Figure 3.

An exclusive small signal model for the proposed TIA design is envisaged in Figure 4. Values such as g_{mbx} were included implicitly, however, it is important to point out that values such as r_{dsx} , C_{dx} , C_{gx} were not possible to ignore. The effect of Miller parasitic capacitances involving C_{gd1} and C_{gd3} was minimal. Enough headroom was provided for the gate-source voltages for transistor M_1 and M_3 which enabled better transconductance parameters for these amplifying transistors as follows in

TABLE 1. W/L aspect ratio for NMOS and PMOS transistors used in this work

Ref. M_x	M_1	M_2	M_3	M_4	M_5	M_6	M_7
W/L	125	125	50	187.5	40	40	36.9

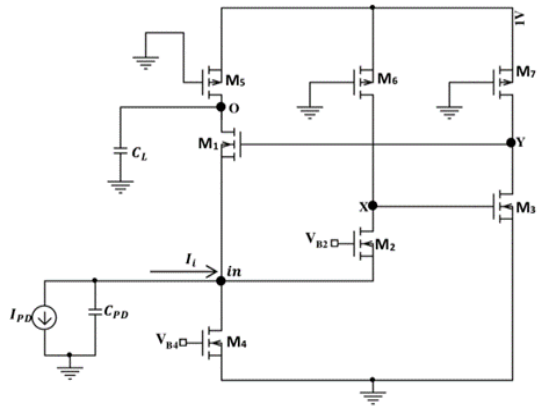

Figure 3. Proposed SPL TIA topology

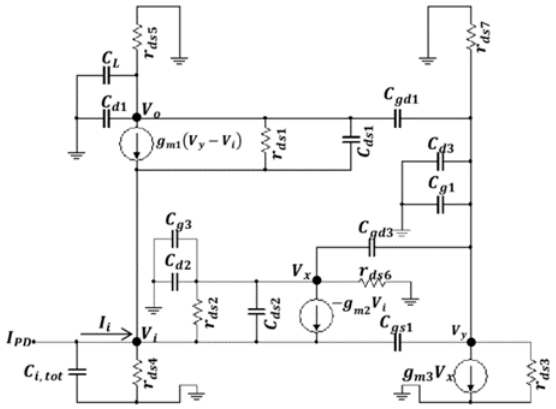

Figure 4. Small signal model of the proposed SPL TIA topology

Table 2. In this table, transconductance parameters for other transistors are also included.

2. 1. 1. Transimpedance Gain Formula

Following on the small signal model of Figure 4, the TIA gain formula can be established. To start with, the voltage gain from the input node to node X. Equations (6)-(8) are with symbolic transconductances parameters g_{mx}, body transconductance g_{mbx} drain-to-source conductances g_{dsx} and drain capacitance C_{dx} of transistor Mx and C_{gx} gate capacitance of transistor Mx (referenced to body ground) shown in Figure 3 is as follows:

$$A_2 = \frac{V_x}{V_i} \approx \frac{g_{m2}+g_{mb2}+g_{ds2}}{g_{ds6}+g_{ds2}+s(C_{d2}+C_{g3})} \quad (6)$$

TABLE 2. Transconductance parameters for transistors M_1 – M_7

Transistor No.	M_1	M_2	M_3	M_4	M_5	M_6	M_7
g_m/mS	5.49	5.80	2.70	9.28	3.20	3.54	1.58

Voltage gain from node X to node Y is represented as:

$$A_3 = \frac{V_y}{V_x} \approx -\frac{g_{m3}}{g_{ds7}+g_{ds3}+s(C_{d3}+C_{g1})} \quad (7)$$

The overall voltage gain of the proposed circuit is:

$$A = \frac{V_o}{V_i} = A_1\left[1 + |A_2A_3| + \frac{1}{g_{m1}}[g_{mb1} + g_{ds1}]\right] \quad (8)$$

In which the voltage gain of transistor M_1 is expressed as:

$$A_1 = \frac{g_{m1}}{g_{ds5}+g_{ds1}+s(C_{d1}+C_L)} \quad (9)$$

It is important to notice that from Equations (6-9), many terms were not possible to neglect. The voltage gain is increased by a factor of $((1 + |A_2A_3|) + (1/g_{m1})(g_{mb1} + g_{ds1}))$ compared to previous literature which was only by a factor of $(1 + |A_2A_3|)$ [9]. Similarly, a much more reduced input impedance is formulized in Equation (10):

$$Z_i = \frac{1}{\beta+sC_{eq}} \quad (10)$$

In which an exclusive formula of β which is the circuit input admittance is obtained as follows,

$$\beta = g_{m1}(1 + |A_2A_3|) + g_{ds2}(1 - A_2) + g_{ds1}(1 - A) + g_{mb1} + g_{m2} + g_{mb2} + g_{ds4} \quad (11)$$

As the equivalent capacitance C_{eq} is influenced by the total input capacitance $C_{i,tot}$ and the unitless magnitude of $|A_2A_3|$ multiplied by gate-to-source capacitance C_{gs1} of transistor M1 as:

$$C_{eq} = [C_{i,tot} + |A_2A_3|C_{gs1}] \quad (12)$$

The DC input resistance is therefore,

$$R_{in_{DC}} = \frac{1}{\beta} \quad (13)$$

Taking into account that the f_{-3dB} TIA bandwidth becomes:

$$f_{-3dB} = \frac{\beta}{2\pi C_{eq}} \quad (14)$$

Leading to the following exclusive TIA gain formula:

$$Z_{TIA} = \frac{A}{\beta+sC_{eq}} \quad (15)$$

A much reduced input impedance with high voltage gain contributing to high TIA gain as in Equation (15).

2. 2. AIL TIA In Figure 5, an active inductor load is presented within the TIA which consists of two PMOS transistors (M_5 and M_8) that have similar aspect ratios (W/L). As for the small signal model, it is similar to that of Figure 4 except for the replacement of r_{ds5} by the active inductor load impedance Z_{AIL} which is expressed as follows [19]:

$$Z_{AIL} = \frac{r_{o8}C_{gs5}s+1}{g_{m5}+C_{gs5}s} \quad (16)$$

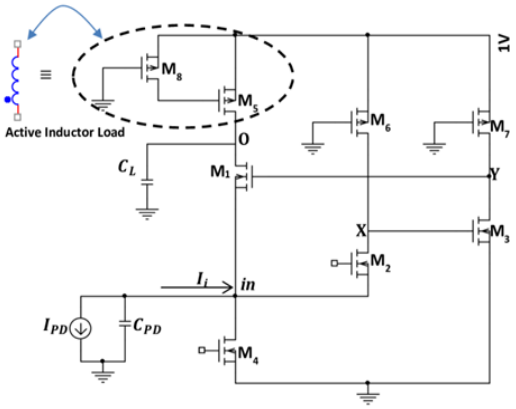

Figure 5. Proposed AIL TIA topology

The AIL admittance Y_{AIL} constitutes a part of the M_1 transistor voltage gain and given the fact that this admittance is of an extremely low value at high frequencies, it is valid to assume that the voltage gain of transistor M_1 has become more dominant within the overall voltage gain A, in contrast with the SPL TIA that had an expression for A_1 given in Equation (9). In the case of the AIL TIA, it is represented as:

$$A_1 = \frac{g_{m1}}{Y_{AIL}+g_{ds1}+s(C_{d1}+C_L)} \quad (17)$$

In fact, high frequency cases lead to situation where $g_{ds1} \gg Y_{AIL}$ as:

$$A_1 \approx \frac{g_{m1}}{g_{ds1}+s(C_{d1}+C_L)} \quad (18)$$

It is therefore important to point out that Equations (8-11) and (13-15) (from previous section) are implicitly influenced by Equation (18). According to extracted data from simulation, compared with SPL TIA, a lower g_{m1} is obtained for the AIL TIA with higher g_{ds1}. This reduction in A_1 leads to lower voltage gain A, eventually lowering TIA gain and bandwidth according to Equations (11), (14) and (15). However, a reduction in the input referred noise current and power consumption do occur. The much reduced drain current I_{D1} in the AIL TIA compared with the SPL TIA is due to having the AIL to be near an open circuit situation at high frequencies (i.e. near ideal current source).

Following on Equation (16) with regard to the active inductor impedance, and in an ideal situation, a pole zero is created to resonate with the output capacitance for the purpose of bandwidth extension. However, in the AIL TIA, the focus is on an input referred noise lowering mechanism through lowering the AIL admittance.

3. NOISE ANALYSIS

3. 1. Noise Analysis of SPL TIA The common formula for the mean square channel thermal noise

voltage (spectral density) at the drain of transistor M_1 is as follows [9]:

$$\overline{V_{no,d1}^2} = 4kT\alpha g_{m1}(Z_{TIA} - Z_o)^2 \quad (19)$$

Where $\alpha = \gamma(g_{d0}/g_m)$, as γ is the channel thermal noise coefficient, g_{d0} is the zero bias drain conductance. A unique formula for the output impedance in this work is as:

$$Z_o = \frac{1}{(g_{ds5}+g_{ds1})+s(C_{d1}+C_L+C_{ds1})} \quad (20)$$

The drain of transistor M_2 mean square channel thermal noise voltage is:

$$\overline{V_{no,d2}^2} = 4kT\alpha g_{m2}\left(Z_{TIA} - Z_x\frac{V_o}{V_x}\right)^2 \quad (21)$$

where the impedance at node X is worked out as:

$$Z_x = \frac{1}{(g_{ds2}+g_{ds6})+s(C_{d2}+C_{g3}+C_{ds2}+C_{gd3})} \quad (22)$$

And the voltage gain from node X to output node O is derived as:

$$\frac{V_o}{V_x} = \frac{A[(g_{ds6}+g_{ds2})+s(C_{d2}+C_{g3})]}{g_{m2}+g_{mb2}+g_{ds2}} \quad (23)$$

The drain of transistor M_3 mean square channel thermal noise voltage is:

$$\overline{V_{no,d3}^2} = 4kT\alpha g_{m3}\left(Z_{TIA} - Z_y\frac{V_o}{V_y}\right)^2 \quad (24)$$

where the impedance at node Y is worked out as:

$$Z_y = \frac{1}{(g_{ds3}+g_{ds7})+s(C_{gs1}+C_{gd3}+C_{g1}+C_{d3}+C_{gd1})} \quad (25)$$

while the voltage gain from node Y to output node O is:

$$\frac{V_o}{V_y} = \frac{Ag_{m1}}{(g_{m1}+g_{mb1}+g_{ds1}-A(g_{ds5}+g_{ds1}))-sA(C_{d1}+C_L)} \quad (26)$$

A modification to previous literature [9] is worked out based on short channel effects literature [15] regarding mean square induced gate noise voltage (spectral density) for transistor M_1 as follows:

$$\overline{V_{no,g1}^2} = 4kT\delta\frac{(\omega C_{gs1})^2}{5g_{d01}}\left(Z_{TIA} - Z_y\frac{V_o}{V_y}\right)^2 \quad (27)$$

In which the shunt conductance g_g is equal to $(\omega C_{gs1})^2/5g_{d01}$which was previously thought to be $(\omega C_O)^2/g_{d01}$, where C_O was given as the gate-oxide capacitance, while g_{d0} is the drain conductance at zero bias [9], given that γ is the channel thermal noise coefficient, while δ is the gate noise coefficient. Similarly, the mean square induced gate noise voltage for transistor M_2 and M_3 is:

$$\overline{V_{no,g2}^2} = 4kT\delta\frac{(\omega C_{gs2})^2}{5g_{d02}}(Z_{TIA})^2 \quad (28)$$

$$\overline{V_{no,g3}^2} = 4kT\delta\frac{(\omega C_{gs3})^2}{5g_{d03}}\left(Z_x\frac{V_o}{V_x}\right)^2 \quad (29)$$

The overall gate and drain noise contribution is defined in common form as [9]:

$$\overline{V_{no,Mx}^2} = \overline{V_{no,dx}^2} + \overline{V_{no,gx}^2} + 2|c|\sqrt{\overline{V_{no,dx}^2}\cdot\overline{V_{no,gx}^2}} \quad (30)$$

where c is the cross correlation coefficient (drain-to-gate noise). The noise voltage contribution of transistor M_4 is defined in this work as:

$$\overline{V_{no,M4}^2} = 4kT(Z_{TIA})^2 g_{ds4} \quad (31)$$

While noise voltage contribution of current sources M_5, M_6 and M_7 is defined in this work as:

$$\overline{V_{no,r}^2} = 4kT\left(Z_o^2 g_{ds5} + Z_x^2 g_{ds6}\left(\frac{V_o}{V_x}\right)^2 + Z_y^2 g_{ds7}\left(\frac{V_o}{V_y}\right)^2\right) \quad (32)$$

And the total integrated mean square noise voltage spectral density contribution is:

$$\overline{V_{no}^2} = \overline{V_{no,M1}^2} + \overline{V_{no,M2}^2} + \overline{V_{no,M3}^2} + \overline{V_{no,M4}^2} + \overline{V_{no,r}^2} \quad (33)$$

And the input referred noise current is given in the following common formula:

$$\overline{I_{in}^2} = \frac{\overline{V_{no}^2}}{(Z_{TIA})^2} \quad (34)$$

3. 2. Noise Analysis of AIL TIA The output impedance representation for the AIL TIA is manifested as:

$$Z_o = \frac{1}{(Y_{AIL}+g_{ds1})+s(C_{d1}+C_L+C_{ds1})} \quad (35)$$

The output impedance is characterized through which $g_{ds1} \gg Y_{AIL}$ and so as the voltage gain from node Y to output node O is:

$$\frac{V_o}{V_y} = \frac{Ag_{m1}}{(g_{m1}+g_{mb1}+g_{ds1}-A(Y_{AIL}+g_{ds1}))-sA(C_{d1}+C_L)} \quad (36)$$

Then having an exclusive formula as:

$$\frac{V_o}{V_y} = \frac{Ag_{m1}}{(g_{m1}+g_{mb1}+g_{ds1}(1-A))-sA(C_{d1}+C_L)} \quad (37)$$

While noise voltage contribution of current sources M_6 and M_7 and the active inductor load noise voltage contribution is defined uniquely in this work as:

$$\overline{V_{no,r}^2} = 4kT\left(Z_o^2 Y_{AIL} + Z_x^2 g_{ds6}\left(\frac{V_o}{V_x}\right)^2 + Z_y^2 g_{ds7}\left(\frac{V_o}{V_y}\right)^2\right) \quad (38)$$

It is noticed that the term $Z_o^2 Y_{AIL}$can be neglected given what was stated before regarding an extremely low active inductor admittance and this concept explains a significant reduction in the overall input referred noise

compared to the SPL TIA. Bearing in mind that the TIA gain has changed in nature compared with the SPL TIA, however, the rest of formulas remained unchanged. In Equation (36), the term $A(Y_{AIL}+g_{ds1})$ is also reduced, leading to reduction in the voltage gain from node Y to output node O (i.e V_o/V_y) , hence lowering the magnitude of the term $Z_y^2 g_{ds7}(V_o/V_y)^2$ in Equations (37-38).

4. COMBINED TIAs RESULTS AND DISCUSSION

In simulation, the SPL TIA has a transimpedance gain of 51.16 dBΩ at f_{-3dB} bandwidth of 20.16 GHz as in Figure 6. The point of f_{-3dB} bandwidth is in total agreement with Equation (14). From Equation (15), transimpedance gain is proportional to voltage gain through which signal gain A_1 is extended by a factor of $\left(1+|A_2A_3|+\frac{1}{g_{m1}}[g_{mb1}+g_{ds1}]\right)$ according to Equations (8-9) that had an important impact. However, a greater extension of β as in Equation (11) could not affect the total TIA gain, while it serves in input impedance lowering mechanism. A slight capacitive peaking appears around 10 GHz, while in comparative work literature [9], it shows clear capacitive peaking well beyond 10 GHz. In an AIL TIA, a transimpedance gain of 42.7 dBΩ is achieved with f_{-3dB} bandwidth of 3.75 GHz. A transimpedance phase shift of 58.4° at the point of f_{-3dB} bandwidth is illustrated in Figure 7 for the SPL TIA, while it was 132.1° for the AIL TIA.

The TIA gain in terms of ohmic resistance is manifested in Figure 8 with 362.3 Ω at the point of f_{-3dB} bandwidth. Very limited ohmic gain peaking appears below 10 GHz which is well below the dominant pole. In the AIL TIA, a 136.5 Ω of TIA gain at the point of bandwidth is obtained.

The DC optimal supply voltage was applied at 1V for the SPL and the AIL TIAs. A range of supply voltages (0.9V-1.1V) were applied in Figure 9 in relation to TIA gain. A much more reduced bandwidth occurred at 0.9V, while the supply voltage of 1.1V happened to slightly extend the bandwidth at the expense of power consumption with slight reduction in SPL TIA gain. In Figure 10, a big TIA gain gap appeared in the AIL TIA between the DC biasing of 1.1V and the rest of DC biasing (0.9V, 1V) in which there was a limited shift if any with regard to the bandwidth. In Figure 11, a temperature sweep from 20°C-60°C was run to examine how the SPL TIA gain is influenced, while the bandwidth is not dramatically shifted. However, from the input

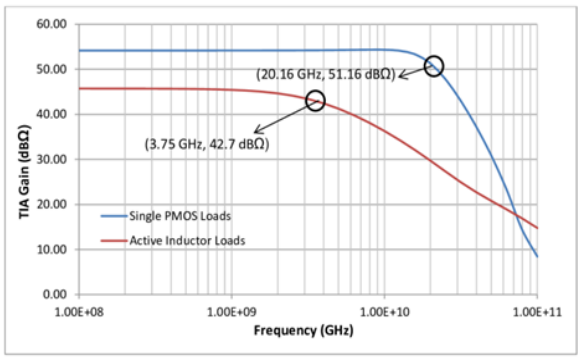

Figure 6. Simulated transimpedance gain in dBΩ unit

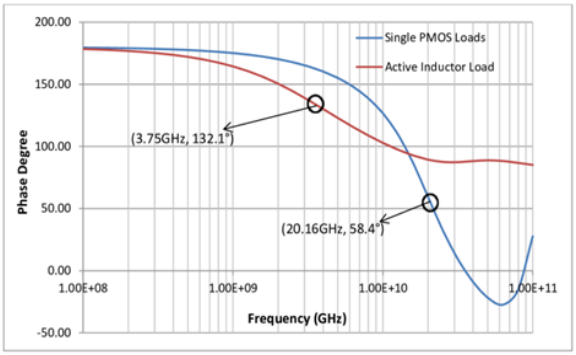

Figure 7. Transimpedance phase shift versus frequency relationship

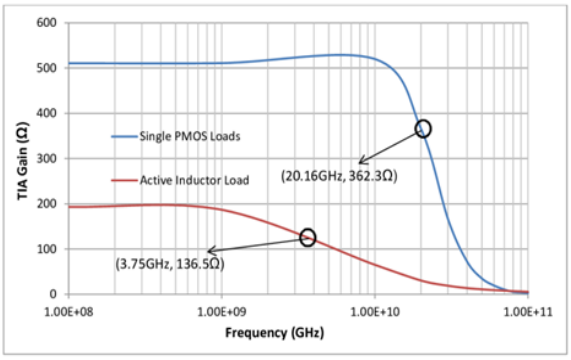

Figure 8. Simulated transimpedance gain in ohmic unit

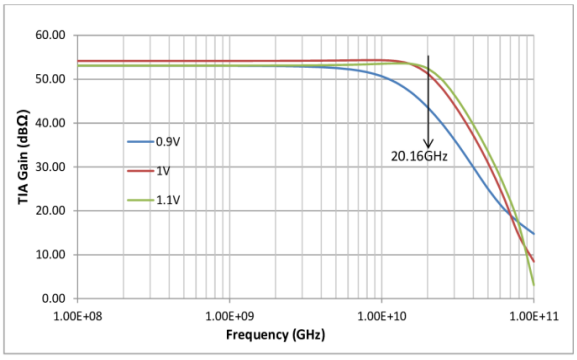

Figure 9. DC supply voltage sweep from 0.9 V–1.1 V with relationship to gain for SPL TIA

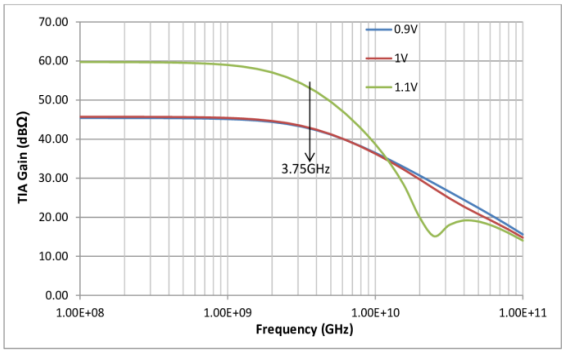

Figure 10. DC supply voltage sweep from 0.9 V–1.1 V with relationship to gain for AIL TIA

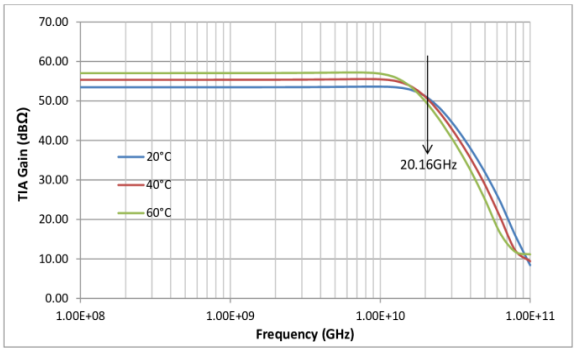

Figure 11. Temperature sweep from 20°C - 60°C in relation to gain for SPL TIA

referred noise current point of view, a rapid increase is expected at higher temperatures. A wider gap in TIA gain appeared in temperature sweep from 20°C-60°C for the AIL TIA as in Figure 12.

The input impedance of the SPL TIA shown in Figure 13 indicates low values in which at the point of f_{-3dB} bandwidth, a simulated value of 43.6 Ω was obtained. Capacitive peaking does appear beyond 10 GHz as it is possible in this case to have the dominant pole below the input impedance pole. The input impedance of the AIL TIA indicated a value of 128.2 Ω at the point of bandwidth.

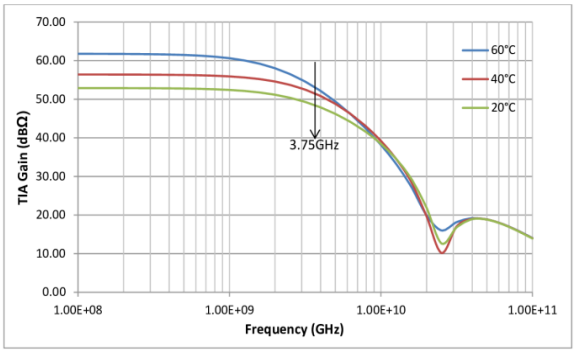

Figure 12. Temperature sweep from 20°C - 60°C in relation to gain for AIL TIA

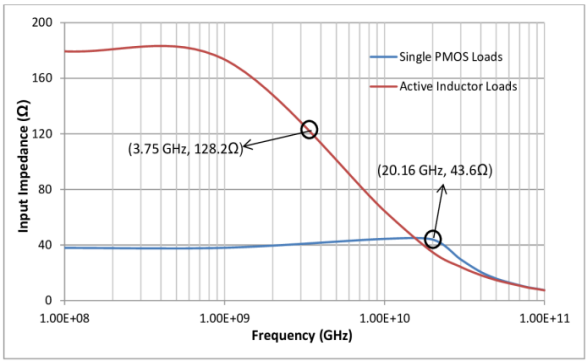

Figure 13. Input impedance of the proposed TIAs circuit based on simulated data

From an extracted data (from simulation) for the DC transfer function, I_{PD} input impedance as well as the output impedance at V_{out} are illustrated in Table 3. The DC transfer function for the AIL TIA is given in Table 4.

In Figure 14, a 20 Gb/s 2^{31}-1 NRZ PRBS eye diagram for the SPL TIA is simulated, in which for an input signal of 100 µA, with nonlinear simulation of 1 µs stop time and maximum time step of 13 ps. The amount of distortion (set by the signal-to-noise ratio) was about 8 mV, while the signal-to-noise ratio at the sampling point was 57 mV. Best time to sample (decision point) was at 43 ps which is the most open part of the eye (best signal-to-noise ratio) and the measure of jitter was 6.7 ps. In Figure 15, a 3.5 Gb/s 2^{31}-1 NRZ PRBS eye diagram for the AIL TIA is simulated. A nonlinear time-domain simulation with 7 µs stop time and a maximum time step of 5 ps was performed. An input signal of 100 µA was applied in which the amount of distortion in the eye diagram was around 1 mV and the signal-to-noise ratio at the sampling point was 18 mV. The decision point was at 283 ps and the measure of jitter was 4 ps.

In Table 5, a simulation extraction of total power consumption of 1.052 mW partitioned as per each transistor in the SPL TIA, while the total power consumption was 0.66 mW in the AIL TIA as in Table 6.

TABLE 3. Extracted data from simulation for the SPL TIA

DC Transfer Function	-510.743
I_{PD} Input Impedance	37.95 Ω
Output impedance at V_{out}	624.20 Ω

TABLE 4. Extracted data from simulation for the AIL TIA

DC Transfer Function	-193.304
I_{PD} Input Impedance	179.514
Output impedance at V_{out}	496.828

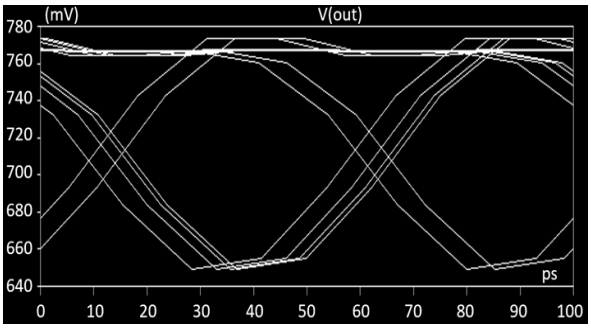

Figure 14. Screen shot of eye diagram for 20 Gbps bit sequencing for the SPL TIA

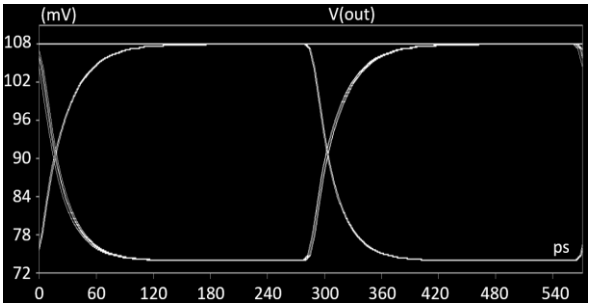

Figure 15. Screen shot of eye diagram for 3.5 Gbps bit sequencing for the AIL TIA

TABLE 5. A simulation extraction of total power consumption of 1.052 mW partitioned as per each transistor for the SPL TIA

Power Consumption mW	Transistor No.
0.259	$\mathbf{M_1}$
0.259	$\mathbf{M_2}$
0.190	$\mathbf{M_3}$
0.101	$\mathbf{M_4}$
0.093	$\mathbf{M_5}$
0.11	$\mathbf{M_6}$
0.028	$\mathbf{M_7}$

TABLE 6. A simulation extraction of total power consumption of 0.66 mW partitioned as per each transistor for the AIL TIA

Power Consumption mW	Transistor No.
9e-6	$\mathbf{M_1}$
0.273	$\mathbf{M_2}$
0.2	$\mathbf{M_3}$
0.045	$\mathbf{M_4}$
0.002	$\mathbf{M_5}$
0.105	$\mathbf{M_6}$
0.033	$\mathbf{M_7}$
1e-4	$\mathbf{M_8}$

The simulated input referred noise current spectral density for the SPL TIA is shown in Figure 16 in which 34.4 $pA/\sqrt{Hz}$ at the f_{-3dB} bandwidth (20.16 GHz) was reported. This result is quite important given the fact that the TIA gain was 51.16 dBΩ with a 362.3 Ω transimpedance in terms of ohmic resistance at 1V DC supply voltage with a power consumption of only 1.052 mW. The reported input referred noise current overcomes the drawbacks associated with the common gate amplifiers in which the thermal noise of the load resistor and the biasing network are basically referred back directly with unity gain [17-18]. As for the AIL TIA, an input referred noise of 21.4 $pA/\sqrt{Hz}$ at the point of bandwidth (3.75 GHz) was obtained.

4. 1. SPL Versus Inductor Loads The PMOS transistors loads M_5, M_6 and M_7 represent an extremely high small-signal resistance (ideally near infinite) having parallel r_{o5}, r_{o6} and r_{o7} resistances respectively in which for instance, the voltage gain of the common source transistor M_3 equals $(-g_{m3}r_{o3})$ as compared to the case where an inductive load Ls is present as in literature [9]. Despite the channel length modulation involved, a stable path for drain currents via transistors loads M_5, M_6 and M_7 is secured in which these drain currents are far less dependent on the voltages at nodes O, X and Y, in contrast with inductor loads voltage transients dependence on di/dt. The voltage gain of the mentioned common source stage represents the highest gain possible for a single transistor. Consequently, the trade-off between voltage gain and signal headroom can be eased when a PMOS load is introduced instead of an inductive load. Ultimately, PMOS transistor loads M_5, M_6 and M_7 will simply behave like a resistor, each resistor is exactly similar to the output resistance of the PMOS transistor given a constant gate-to-source voltage for each transistor. In addition to high voltage gain, the TIA gain with PMOS considerably depends on β, as in Equation (15), unlike the situation of inductor load where it depends mainly on the real part of the inductor load admittance.

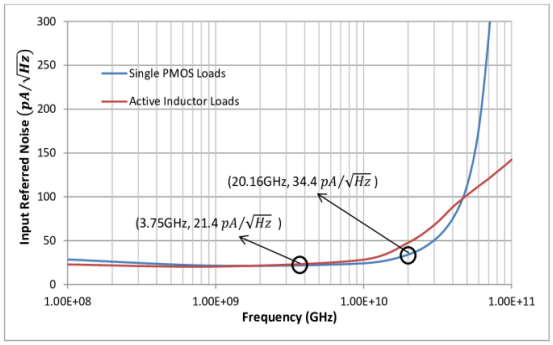

Figure 16. Input referred noise current spectral density based on simulated data

The PMOS current source load can improve SPL TIA performance since it enhances the TIA gain, while it does not suffer from the drawbacks of the inductor load especially when it comes to enabling NMOS transistors M_1, M_2 and M_3 to consume less power in contrast with actual inductor loads stated in previous literature [9]. Less thermal resistivity in NMOS transistors constitute less noise contribution. Conductances g_{ds5}, g_{ds6} and g_{ds7} in Equation (32) are optimized to have low enough values to reduce noise contribution through channel length modulation, while series resistances with inductor loads do not have this capability since the inductor loads are already a source of dissipating energy into the amplifier NMOS transistors in a form of thermal resistivity.

Comparative analysis between SPL TIA and inductor load TIA [9] in the feedforward structure show that the inductor load suffer from unclamped inductive switching which means that there is an absence of what is known as a "freewheeling'' diode for discharging energy especially when the input signal of NMOS transistors M_1 , M_2 and M_3 is in the lower state (from small signal point of view), essentially meaning that all the energy is dissipated into these transistors. Through inductance, current is rapidly turned off, while the magnetic field cannot respond and therefore, does not collapse instantaneously. As a result, an induced electromagnetic force (a counter one) can surprisingly accumulate high potential over the switching NMOS in which this potential is proportional to the speed through which the current is extremely low. Furthermore, inductor load may cause the NMOS transistors M_1, M_2 and M_3 to breakdown at low signal state due to stray capacitance (from drain to gate), while the ability of these NMOS transistors to withstand energy (thermal resistivity) is put into question. Signal switching from high to low state in the inductor load generate high voltage transients in which they can be coupled into the NMOS transistors gates through their stray capacitors C_{gd} causing damage.

4. 2. AIL Versus Inductor Load In Figure 5, parasitic capacitor C_{gs5} acts as an open circuit at low frequencies in which transistor M_5 effectively becomes diode-connected as the active inductor impedance given in Equation (16) becomes $Z_{AIL} = 1/g_{m5}$. At high frequencies however, the gate of M_5 is at ac ground in which $Z_{AIL} \approx r_{o8}$. Since r_{o8} only depends on channel length modulation and drain current, there is no possible current transients as in the case of inductor loads, hence there is no dissipation of energy into transistor M_1 (i.e less noise contribution). Apart from the fact that tuning the active inductor part is much more accurate (than an inductor load) by tuning the equivalent inductance for the purpose of realizing high frequency inductive impedance. In this work, since $r_{o8} \gg 1/g_{m5}$, the equivalent inductance is:

$$L_{eq} = \frac{r_{o8}C_{gs5}}{g_{m5}} \quad (39)$$

The power consumption reduction from 1.052 mW in SPL TIA to 0.66 mW in AIL TIA is due to the high frequency AIL impedance $Z_{AIL} = r_{o8}$ which enables higher voltage drop that approximates near ideal current source. From transistors M_6 and M_7 side view, the active inductor load deprives them from significant level of drain current and drives them into deep triode region. Consequently, it is just about enough voltage headroom for transistors M_2 and M_3 to operate.

4. 3. Comparative TIA Performance Analysis A comparative TIA performance analysis show that in this work, an extremely low power consumption and input referred noise with inductor less design, and wide bandwidth to considerable extent with reasonably good TIA gain using 1V DC supply voltage are illustrated in Table 7 which displays various performance analyses in relation to this work. The power consumption of the proposed TIA design is below half of that reported in

TABLE 7. A comparative performance analysis with other TIA topologies

No. of Inductors	Input Referred Noise $\left(\frac{pA}{\sqrt{Hz}}\right)$	Bandwidth (GHz)	TIA Gain dBΩ	DC Supply Voltage (V)	Power Consumption (mW)	CMOS Technology (nm)	Year	Ref.
2	30	26.1	46.7	1.2	8.2	65	2010	[10]
8	31	70	40	1.2	24	65	2014	[11]
7	2.5 μA_{rms}	40	55	1.6	107	65	2014	[12]
0	20.3	7	40.5	1	1.4	90	2018	[22]
3	**50**	**20**	**52**	**1**	**2.2**	**80**	**2004**	[9]
0	**34.3**	**20.16**	**51.16**	**1**	**1.052**	**65**	**2021**	**This Work SPL TIA**
0	**21.4**	**3.75**	**42.7**	**1**	**0.66**	**65**	**2021**	**This Work AIL TIA**

literature [9] in SPL TIA and is well below that in the AIL TIA. The input-referred noise current spectral density is considerably lower compared to same literature, while maintaining near levels in terms of TIA gain and bandwidth in the SPL TIA for 1V DC supply voltage. In the AIL TIA, despite of lower TIA gain and bandwidth, it registered a considerable reduction of input referred noise current and power consumption. Interestingly, budget DC supply voltage in literature within Table 7 ranged from 1.6V down to 1V (only 0.6V difference) and subsequently power consumption was reduced from 107 mW down to just 0.66 mW despite various design processes involved with moderate change in TIA gain. The rate of change in bandwidth is well below that of power consumption and that is expected. The common feature in various design topologies, device discrete dimensions and processes stated in literatures is that they all face short channel effects challenges as in Equation (5) in which mosfets depart from classic saturation condition square law and enter into $\theta(V_{gs} - V_{th}) \neq 0$. Nevertheless, the input referred noise current spectral density for instance maintained (in this work) its obvious comparable results. Ordinary spiral inductor presence in numbers deepens the trade-off gap especially in terms of gain and power consumption as reported in literature [12].

5. CONCLUSION

The major contribution of this work is that inductor loads may not be the best suitable solution for improving TIA circuit performance, while single PMOS current source loads in feed forward TIA topology proved to be the best compromise for the trade-off in power consumption, input referred noise current spectral density, with wide bandwidth, high transimpedance gain and low DC supply voltage. The AIL TIA have shown to have a challenging very low input referred noise and power consumption (instead of inductor loads), while maintaining relatively moderate TIA gain at a bandwidth suitable for many applications.

6. FUTURE SCOPE

The overcoming of classical inductor load peaking problems offers a new way of introducing active loads and active inductor loads in a manner that has not been possible before. In addition, an introduction of an active inductor which is embedded in a form of negative feedback loop (shunt-shunt feedback) is an interesting way to follow.

7. REFERENCES

1. Seifouri, M., Amiri, P. and Rakide, M., "Design of broadband transimpedance amplifier for optical communication systems", ***Microelectronics Journal***, Vol. 46, No. 8, (2015), 679-684, https://doi.org/10.1016/j.mejo.2015.05.007
2. Lee, J., Park, H.G., Kim, I.S., Pu, Y., Hwang, K.C., Yang, Y., Lee, K.-Y. and Seo, M., "A 6 gb/s low power transimpedance amplifier with inductor peaking and gain control for 4-channel passive optical network in 0.13 μm cmos", ***JSTS: Journal of Semiconductor Technology and Science***, Vol. 15, No. 1, (2015), 122-130, https://doi.org/10.5573/JSTS.2015.15.1.122
3. Taghavi, M.H., Naji, A., Belostotski, L. and Haslett, J.W., "On the use of multi-path inductorless tias for larger transimpedance limit", ***Analog Integrated Circuits and Signal Processing***, Vol. 77, No. 2, (2013), 221-233, https://doi.org/10.1007/s10470-013-0140-9
4. Zhenghao, L., Dandan, C. and Seng, Y.K., "An inductor-less broadband design technique for transimpedance amplifiers", in Proceedings of the 2009 12th international symposium on integrated circuits, IEEE., (2009), 232-235.
5. Atef, M., Aznar, F., Schidl, S., Polzer, A., Gaberl, W. and Zimmermann, H., "8 gbits/s inductorless transimpedance amplifier in 90 nm cmos technology", ***Analog Integrated Circuits and Signal Processing***, Vol. 79, No. 1, (2014), 27-36, https://doi.org/10.1007/s10470-013-0242-4
6. Atef, M. and Zimmermann, H., "Low-power 10 gb/s inductorless inverter based common-drain active feedback transimpedance amplifier in 40 nm cmos", ***Analog Integrated Circuits and Signal Processing***, Vol. 76, No. 3, (2013), 367-376, https://doi.org/10.1007/s10470-013-0117-8
7. Kim, S.H., Cho, S.B. and Park, S.M., "Dual-mode cmos feed-forward transimpedance amplifier for ladars", ***Electronics Letters***, Vol. 50, No. 23, (2014), 1678-1680, https://doi.org/10.1049/el.2014.2678
8. Chen, R.Y. and Yang, Z.-Y., "Cmos transimpedance amplifier for visible light communications", ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems***, Vol. 23, No. 11, (2014), 2738-2742, doi: 10.1109/TVLSI.2014.2365462.
9. Kromer, C., Sialm, G., Morf, T., Schmatz, M.L., Ellinger, F., Erni, D. and Jackel, H., "A low-power 20-ghz 52-db/spl omega/transimpedance amplifier in 80-nm cmos", ***IEEE Journal of Solid-State Circuits***, Vol. 39, No. 6, (2004), 885-894, doi: 10.1109/JSSC.2004.827807.
10. Bashiri, S., Plett, C., Aguirre, J. and Schvan, P., "A 40 gb/s transimpedance amplifier in 65 nm cmos", in Proceedings of 2010 IEEE international symposium on circuits and systems, IEEE., (2010), 757-760.
11. Ahmed, M.N., Chong, J. and Ha, D.S., "A 100 gb/s transimpedance amplifier in 65 nm cmos technology for optical communications", in 2014 IEEE International Symposium on Circuits and Systems (ISCAS), IEEE., (2014), 1885-1888.
12. Ding, R., Xuan, Z., Baehr-Jones, T. and Hochberg, M., "A 40-ghz bandwidth transimpedance amplifier with adjustable gain-peaking in 65-nm cmos", in 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), IEEE., (2014), 965-968.
13. Alatwi, A.M., Rashed, A.N.Z. and Abd El Aziz, I.A., "High speed modulated wavelength division optical fiber transmission systems performance signature", ***Telkomnika (Telecommunication Computing Electronics and Control)***, Vol. 19, No. 2, (2021), 380-389, doi: 10.12928/TELKOMNIKA.v19i2.16871.

14. Dey, A., Nandi, S. and Sarkar, M., "Security measures in iot based 5g networks", in 2018 3rd International Conference on Inventive Computation Technologies (ICICT), IEEE. (2018), 561-566.
15. Ashrafian, A., Mohammad-Taheri, M., Naser-Moghaddasi, M., Khatir, M. and Ghalamkari, B., "Planar circuit analysis of ultra-wideband millimeter-wave inductor using transmission line sections", ***International Journal of Circuit Theory and Applications***, Vol. 49, No. 10, (2021), 3378-3393, https://doi.org/10.1002/cta.3070
16. Hsieh, H.-H., Wu, P.-Y., Jou, C.-P., Hsueh, F.-L. and Huang, G.-W., "60ghz high-gain low-noise amplifiers with a common-gate inductive feedback in 65nm cmos", in 2011 IEEE Radio Frequency Integrated Circuits Symposium, IEEE. (2011), 1-4.
17. Razavi, B., "Design of integrated circuits for optical communications, John Wiley & Sons, (2012).
18. Razavi, B., *Design of analog cmos integrated circuit tata mcgraw*. 2001, Hill.
19. Zohoori, S. and Dolatshahi, M., "A low-power cmos transimpedance amplifier in 90-nm technology for 5-gbps optical communication applications", ***International Journal of Circuit Theory and Applications***, Vol. 46, No. 12, (2018), 2217-2230, https://doi.org/10.1002/cta.2565

Persian Abstract

چکیده

مجموعه ای از بارهای سلف ممکن است بهترین معیار طراحی برای بهبود عملکرد مدار نباشد. در این کار، بهترین مصالحه تاکنون برای مبادله در مصرف برق، چگالی طیفی جریان نویز ارجاعی ورودی، با پهنای باند وسیع، بهره ترانس‌مپدانس بالا و ولتاژ منبع تغذیه DC پایین گزارش شده است. یک تقویت‌کننده ترانس‌مپدانس پیش‌خور CMOS 65 نانومتری شبیه‌سازی‌شده با یک سری بارهای PMOS منفرد به جای یک سری بارهای سلف معرفی شده است. پهنای باند ۲۰.۱۶ گیگاهرتز با بهره ترانسیمپدانس ۵۱.۱۶ dBΩ، تراکم طیفی جریان نویز ورودی ۳۴.۳ p A/√Hz، مصرف برق ۱.۰۵۲ مگاوات و با ولتاژ منبع تغذیه ۱ ولت DC ارائه شده است. علاوه بر این، یک بار سلف فعال (به‌جای بار سلف) در تقویت‌کننده ترانسیمپدانس پیش‌خور CMOS 65 نانومتری معرفی می‌شود. پهنای باند ۳.۷۵ گیگاهرتز با بهره ترانسیمپدانس ۴۲.۷ dBΩ، تراکم طیفی جریان نویز ورودی ۲۱.۴ p A/√Hz، مصرف برق ۰.۶۶ میلی‌وات و با ولتاژ منبع تغذیه ۱ ولت DC گزارش شده است. این فرآیند طراحی پیشخور CMOS 65 نانومتری به دلیل افت ولتاژ DC کمتر در بارهای PMOS، ولتاژ کافی را برای پایانه های گیت به منبع در ترانزیستورهای تقویت کننده فراهم می کند. در نتیجه، این فرآیند طراحی کمترین مصرف توان ممکن را به خصوص با بارهای تک PMOS و همچنین با بار سلف فعال مصرف می کند.