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Modified Second Order Generalized Integrator-frequency Locked Loop Grid Synchronization for Single Phase Grid tied System Tuning and Experimentation Assessment

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ABSTRACT

The phase-locked loop (PLL) is applied in grid-tied systems to synchronise converter operation with grid voltage, affecting converter stability and performance. Synchronous reference frame PLL (SRF-PLL) is a popular grid synchronisation method due to its simplicity and reliability. Normal SRF-PLL cannot suppress DC offset, causing basic frequency and phase oscillations. When a grid is irregular, its bandwidth should be reduced to ensure acceptable disturbance rejection without sacrificing detection speed. To enhance the phase-angle estimation speed and accuracy, the researchers modified structure by adding the pre/in-loop filter in advanced PLLs. The capacity to deliver improved dynamic response and reduced settling time without compromising system stability or the ability to eliminate disturbances is a major issue for PLLs. Among different control methods, SOGI-FLL (second-order generalised integrator-based frequency locked loop) had the best performance. It tracks grid voltage frequency precisely even when there is harmonics, voltage variations, frequency fluctuations, etc. In the event of a dc offset, the calculated frequency incorporates low frequency oscillations. A modified second-order generalised integrator frequency-locked loop (MSOGI-FLL) is presented in this work to address grid voltage anomalies of all types, including dc offset. Using the Waijung Block-set of MATLAB/Simulink, a Modified SOGI-FLL is realized and evaluated by applying abnormal grid voltage situations using a low-cost DSP-based STM32F407VGT microcontroller. The results demonstrate MSOGI-better FLL's performance in harsh circumstances.

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1. INTRODUCTION

Many grid-connected inverters have drawn interest for their economical circuit architecture and advanced control techniques due to the rapid rise in renewable energy [1]. The phase-locked loop (PLL) is an important component in the grid assisted inverter's control strategy since it is primarily utilised to keep the inverter and grid synchronised. A new energy power system's security and stability are directly associated with the performance of the grid-connected inverter [2]. For the converter to work properly, the control algorithm must accurately compute the amplitude, phase-angle, and frequency from the grid voltages. It is difficult when the grid voltage has irregularities(frequency variation, harmonics, voltage fluctuation, dc offset, and/or distortion, switching notches, etc.) [2]. These anomalies can cause measurement and data translation mistakes, making predicting frequency and synchronisation problematic [3]. A phase-locked loop is composed of a phase detector, a filter, and a voltage-regulated oscillator. The PD controls the gain of a voltage-regulated oscillator, whose output signal is frequency and phase synced with the input reference signal. Golestan et al. [3, 4] addressed the categorization of phase lock loop with varying phase detector. Under distorted grid signal

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circumstances, PD structures based on generalised integrators (GI) function better and are more reliable [4, 5]. Thus, SOGI-PLL is better than other PLL designs [3-5]. It works quickly and accurately in bad grid circumstances. In contrast to SOGI-PLL, where the estimated frequency is utilized as feedback from the SOGI-OSG block, SOGI-FLL use a frequency-locked loop (FLL) to adaptively get the frequency [6]. The adaptive nature prevents PLL and improves performance. Factors including transformer nonlinearity, A/D conversion error, analogue device anomalous temperature, and zero drift all produce DC offset when the power grid failure occurs [7, 8]. There are several ways to reduce the DC offset in SRF-PLL nowadays. Golestan et al. [9] suggested a cascaded second-order generalised integrator-phase lock loop (CSOGI-PLL) to eliminate the DC quantity; however, it comprises se Factors including transformer nonlinearity, A/D conversion error, analogue device anomalous temperature, and zero drift all produce DC offset when the power grid failure occurs. It utilizes several SOGI structures, thus the added computing cost is significant [10]. To speed up DC offset removal, Kulkarni et al. [10] devised a cascade delay signal cancellation PLL technique (CDSC-PLL), while Parag et al. [11] utilised an adaptive filter delay signal cancellation-PLL (APF-DSC-PLL) to increase the speed of DC offset rejection, but the complex structure reduces the dynamic performance of the system. Moreover, a phase-locked loop based on the modified delay signal cancellation-PLL was presented by Li et al. [12] which can enhance dynamic performance by reducing DC offset, but it would induce phase deviation, which necessitates design correction. These notch filter (NF) based on PLL and dq-DSC -PLL, as well as five additional approaches for eliminating the DC offset in the PLL. However, these phase detection approches suffer from a sluggish dynamic performance [13-15]. These approaches have the potential to increase dynamic performance while overcoming the drawbacks of conventional low-pass filters [9-16]. However, selecting and calculating the sliding window width is time-consuming [15, 16]. Thus, a modified SOGI-FLL (MSOGI-FLL) for single-phase systems is suggested to reduce frequency estimation errors caused by DC quantity and other grid irregularities (e.g. harmonics, frequency fluctuation, magnitude variation). Using the third integrator as a DC offset cancellation block, the proposed MSOGI-FLL estimates the DC offset without influencing frequency estimation in the FLL.The better performance of this structure has been demonstrated through modelling and experimental findings. The next sections describe the MSOGI-FLL and its performance under various situations.

2. ORGANIZATION & TRANSFER FUNCTION: SECOND-ORDER GENERALIZED INTEGRATOR (SOGI)-FREQUENCY LOCKED LOOP(FLL)

SRF based PLL uses an additional voltage-controlled oscillator, although SOGI-QSGs serve as filters as well as voltage-controlled oscillators. The SOGI resonator's centre frequency is adjusted to match the input frequency using an auto tune block, as shown in Figure 1. The Frequency-Locked Loop (FLL) block estimates the frequency adaptively by changing the gain (Γ) in SOGI-FLL, thus the PLL block used in SOGI-PLL is omitted. The SOGI-FLL works far better, faster, and more accurately than traditional SRF-PLL-based systems in grid anomalies including harmonics, voltage variations, frequency fluctuations, and phase jump etc. for instance. The transfer functions of band-pass filter (BPF) and low-pass filter (LPF) illustrated in Equations (1) and (2) are derived from the conventional SOGI-QSG in Figure 1. A real positive value of gain k can be tuned to alter the bandpass filter $D_{SOGI-FLL}$and low-pass filter $Q_{SOGI-FLL}(s)$bandwidth (or sharpness). This means that the signals Y(s) and Y'(s) are the BPF and LPF outputs, with a 90° phase difference (as shown in bode diagram, Figure 2), respectively. In reality, the LPF outperforms the BPF when it comes to high-frequency filtering. The output signal ($Y'(s)$) of SOGI-QSG is badly affected by a non-zero dc offset in the measured grid voltage.

$D_{SOGI-FLL}(s)$ and $Q_{SOGI-FLL}(s)$ have the following transfer functions:

$$D_{SOGI-FLL}(s) = \frac{Y(s)}{v_{in}(s)} = \frac{k\ s\ \omega}{s^2 + k\omega s + \omega^2} \tag{1}$$

$$Q_{SOGI-FLL}(s) = Q_v(s) = \frac{Y'(s)}{v_{in}(s)} = \frac{k\,\omega^2}{s^2 + k\omega s + \omega^2} \tag{2}$$

Furthermore, Bode's magnitude responses retain 0 dB at the 50Hz fundamental frequency while attenuating amplitude at the 5th and 7th harmonic frequencies of 250Hz and 350Hz, respectively. It should react as a notch filter with zero gain and 180° phase leap at centre frequency to produce auto-tunable SOGI-QSG (see Figure 3).

The transfer function of voltage error signal $\mathbf{E_{SOGI-FLL}}$ can be described as:

$$E_{SOGI-FLL}(s) = E_v(s) = \frac{\varepsilon_{v(s)}}{v_{in(s)}} = \frac{s^2 + \omega^2}{s^2 + k\omega s + \omega^2} \tag{3}$$

In the SOGI-FLL, a frequency error signal (ε_f) is generated from the product of $\boldsymbol{E_{SOGI-FLL}(s)}$ **&** $\boldsymbol{Q_{SOGI-FLL}(s)}$. As illustrated in Figures 1 and 3, the frequency locking loop may be built utilising the

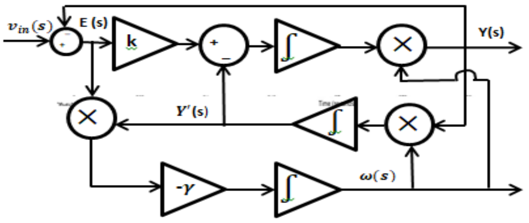
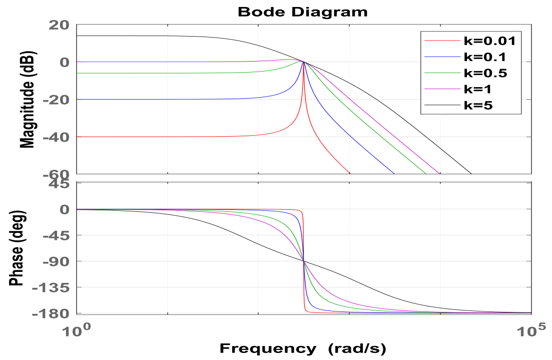


Figure 1. The fundamental architecture SOGI –FLL



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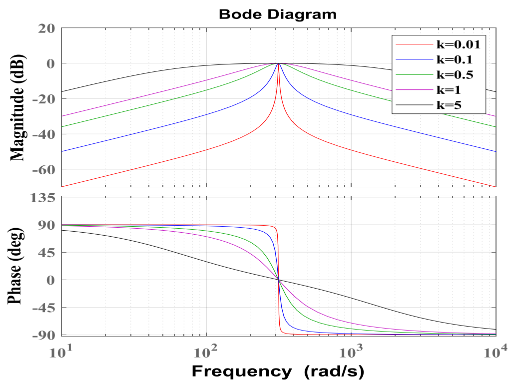


(b)

Figure 2. Bode Graph of (a) $\boldsymbol{D_{SOGI-FLL}(s)}$, and (b) $\boldsymbol{Q_{SOGI-FLL}(s)}$ with various value of k

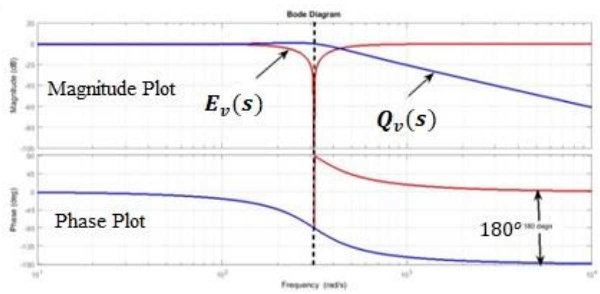


Figure 3. Bode Graph of the $\boldsymbol{E_{SOGI-FLL}(s)}$ & $\boldsymbol{Q_{SOGI-FLL}(s)}$ in an SOGI- QSG

frequency error signal (ε_f) and a negative controller gain($-\gamma$)of frequency loop. The SOGI resonance frequency(ω') is changed until it equals the input frequency (ω) using the frequency loop controller gain ($-\gamma$). A feed-forward variable, ω_c, is included in the FLL to accelerate initial synchronisation. By incorporating feedback, a value of γ should be normalised and defined as follows:

$$\gamma = \frac{k\omega}{V^2}\ \Gamma \tag{4}$$

With a feed-forward of 2π ∗ 50., the dynamic response of frequency estimationin SOGI-FLL is studied. As observed the dynamic response of frequency estimation in Figures 4(a), 4(b), 4(c) and 4(d) using progressive values of k and constant values of γ, and vice versa. Table 1 contains the evaluation of parameter k and γ for SOGI-FLL, as shown in Figure 4 (a)-(d). Transient responsiveness and bandwidth of SOGI-FLL are affected by the para-meter k. The choice of gain k compromises between good signal filtering and transient response of system dynamic responsiveness (Figure 4). The choice of value γ compromises frequency estimate precision and SOGI-FLL dynamics. Reduction in a bandwidth increases rise time (t_{rise} = 0.35/ BW), but improves other metrics.

3. STRUCTURE & TRANSFER FUNCTIONS : MSOGI-FLL

Figure 5 depicts the SOGI-FLL's fundamental structure.

When the third integrator estimates the DC offset, it subtracts it from the signal to improve the system's DC offset rejection capabilities. In addition, Figure 5 shows the suggested MSOGI-FLL structure, which incorporates a DC signal cancellation (DSC) block and a SOGI-FLL structure. In general, a DC-offset can be introduced into the grid signal by the signal conditioning or measuring equipment, as well as other factors like half-wave rectification. Because of this, the pre-filtering stage includes a DC signal cancellation (DSC) block that provides excellent DC-offset rejection and SOGI-FLL rejects the low-order harmonic.

A new version of the band-pass SOGI-FLL (Figure 5) filter [17-19] designated as MSOGI-FLL can be proposed by including the DSC operator. A grid signal polluted with a DC-offset, MSOGI transfer functions is represented as follows for comprehension purposes:

$$D_{MSOGI-FLL}(s) = \frac{Y(s)}{v_{in}(s)} = \frac{k\omega\prime s^2}{s^3 + k\omega'^{s^2} + k'\omega'^{s^2} + \omega'^2 s + k\prime\omega'^3} \tag{5}$$

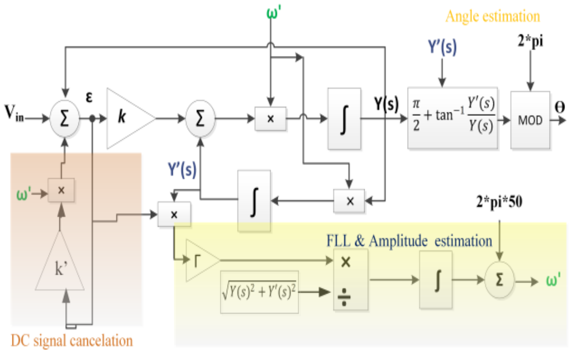


Figure 5. Fundamental architecture of a MSOGI-Frequency lock loop

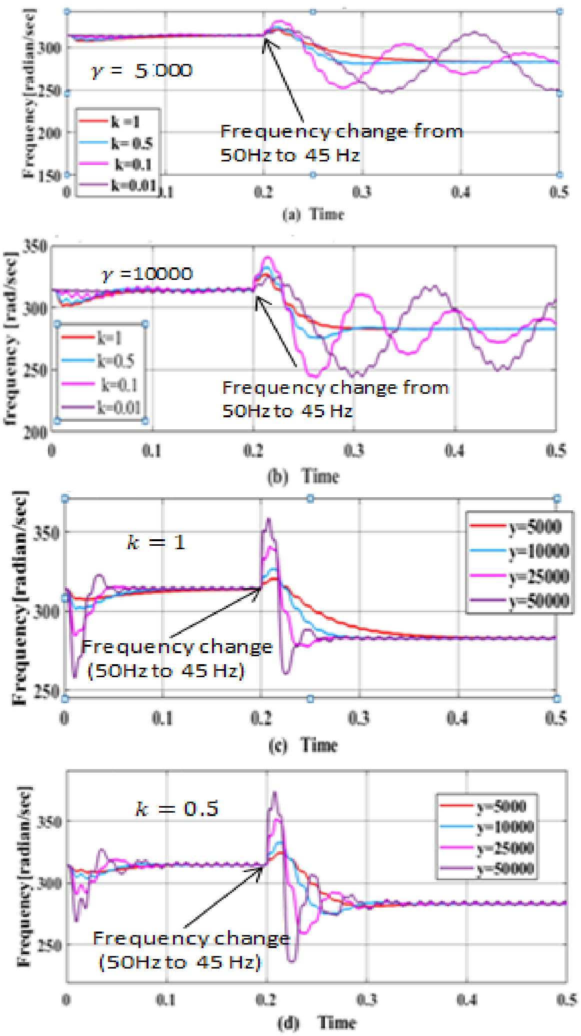


Figure 4. Step response for Frequency Estimation: various values for kand Constant Values (a) γ=5000,(b) γ=10000, (c) &(d)various value of γ and constant value k=1, and k=0.5, respectively

TABLE 1. Evaluation of parameter for SOGI-FLL

Parameter	Variation in parameter	Dynamic response	Steady-state response	Filter response	Settlement time
k	Increase ↑	Worthy	Worthy	Worthy	Reducing
	Decrease↓	Poor	Poor	Poor	Increasing
γ	Increase ↑	Poor	Average	No change	Reducing
	Decrease↓	Worthy	Good	No change	Increasing

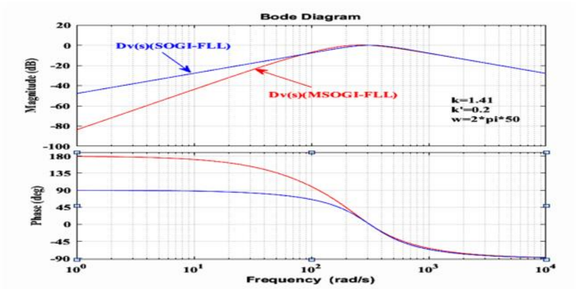
$$Q_{MSOGI-FLL}(s) = \frac{Y'(s)}{v_{in}(s)} = \frac{k\omega' s}{s^3+k\omega' s^2+k'\omega' s^2+\omega'^2 s+k'\omega'^3} \quad (6)$$

$$E_{MSOGI-FLL}(s) = \frac{V_{dc}(s)}{v_{in}(s)} = \frac{k'\omega' s^2+k'\omega'^3}{s^3+k\omega' s^2+k'\omega' s^2+\omega'^2 s+k'\omega'^3} \quad (7)$$

Using Routh hurtiz criteria, the gain k is given as:

$$k = \frac{9.2}{\omega' t_s}\,; t_s = 4.6 * \tau \,; and\ \tau = \frac{1}{\zeta\omega_n} \quad (8)$$

In order to filter out low and high-frequency components in the input signals, gain k must be properly tuned. These graphs (see Figures 2 and 3) show that unlike $D_{SOGI-FLL}(s)$, $Q_{SOGI-FLL}(s)$ attenuates low frequency components, leaving the dc offset.The quantities k and k' are chosen from the roots of the denominator of transfer functions/characteristic equation of MSOGI-FLL($D_{MSOGI-FLL}(s)$, and $Q_{MSOGI-FLL}(s)$) with equal real parts (Figure 6) (all three poles have equal natural frequency of oscillation). On the other hand, ω_{n1} =ω_{n2} =2*pi*50 rad/s (same as for tuning SOGI-FLL) is used to compute the gain k and k' respectively. The bode graphs in Figure 6 demonstrates the impact of both gain adjustments as well as performance assessment of SOGI-FLL and MSOGI-FLL using magnitude plots of transfer functions from equations [1-3] and [5-7]. Figures 6 (a) and 6(b) show magnitude bode graphs of $D_{MSOGI-FLL}(s)$ and $Q_{MSOGI-FLL}(s)$ (Equations 5 and 6), below 0dB for low frequency components, indicating attenuation of low frequency and DC components. It is clear that a positive gain $Q_{SOGI-FLL}(s)$,which does not reduce the DC signal. Due to presence of third generalised integrator, the magnitude of the transfer function $E_{MSOGI-FLL}(s)$ is close to 0dB. Moreover, $Q_{MSOGI-FLL}(s)$ has negative gain at frequencies over 50Hz, which reduces higher order harmonics. But it's considerably lower than50Hz. With the third integrator component (and higher order frequencies) are greatly attenuated, leaving only the low order frequencies to pass, as seen below. It aids in estimating and eliminating the DC offset from grid voltage.



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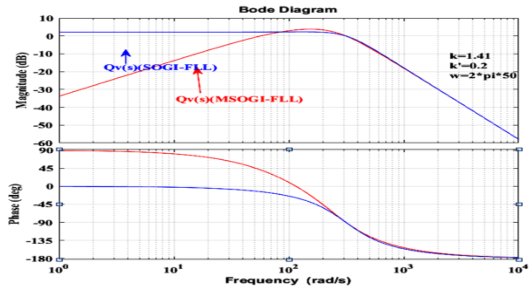

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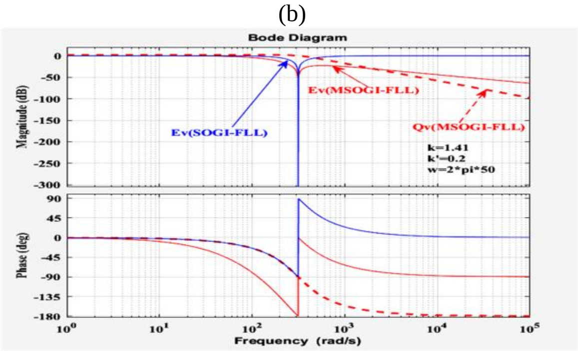


(c)

Figure 6. Bode Graph of the transfer function MSOGI-FLL and SOGI-FLL

4. EXPERIMENTAL RESULTS

MATLAB/ Simulink is used to design and implement the MSOGI-FLL on a downscaled STM32F407VGT6 microcontroller. The discrete MSOGI-FLL model (see Figure 7) is translated to c code before being compiled and dumped into the microcontroller. Microcontroller STM32F407VGT6 has two digital analogue converters (12bit-DAC) and supports waijung environment in SIMULINK/MATLAB (i.e. model-based programming).

It is low cost and 32-bit. Simulated results back up the experimental findings, demonstrating the efficacy of MSOGI-FLL when used in model-based programming There are a few useful parameters for MSOGI-FLL: k = 0,5, k'=0,2,=-5000, sapling time ts = 300 usecond, and f g = 50 Hz for grid voltage frequency. The ADC conversion unit and other digital/discrete units introduce DC-offset, causing inaccuracy in phase estimation of SOGI-FLL.While this was going on, a slew of researchers presented new and better as well ascomplexSOGI-FLL structures of filters. Using the third integrator in MSOGI-FLL to estimate the dc offset allows for better DC offset rejection by subtracting the estimate from the signal. In the experimental setup, MSOGI-FLL is validated by testing each instance separately in the following ways:

Assessment case 1: Experimentation is performed with 0.65p.u. voltage sag on the grid voltage.

Assessment case 2: Examination are performed on grid frequency by imposing a 5% step change (i.e. frequency leap from 50Hz to 45Hz) and a phase angle shift from 0° to 45° on grid frequency and phase.

Assessment 3:grid voltage that has been subjected to harmonic distortion is used.

Figure 8 presents the experimental findings obtained to evaluate the MSOGI-FLL settling time on a grid voltage influenced by a 0.65 p.u voltage sag at Figure 8 depicts the SOGI-FLL v_α / v_{in} settle down near to the fourth cycle, or 45 m-second, when utility voltage is influenced by a voltage drop in grid voltage. A frequency step change from 50Hz to 45Hz and a phase angle shift from 50^0 to 45^0 are applied to the grid voltage during experimental test 2, as illustrated in Figure 9. Only at t =400m-second, as shown in Figure 8, is the phase angle shifted from 50^0 to 45^0. Preliminary results show that the MSOGI-FLL frequency and phase-angle readings are stable, withjust a little frequency shift occurring before the third cycle is reached. This test uses a microcontroller's ADC pin to control the frequency of a sine wave generated inside MATLAB/Simulink (see Figure 7), rather than an AC grid simulator. For experimental test-3, the dynamic response of SOGI-FLL is tested by applying harmonic voltages of 3rd, 5th, and 7th order with amplitudes of 0.35p.u., 0.1p.u., and 0.08p.u. in relation to the fundamental grid voltage (as shown in Figure 10).

As illustrated in Figure 10, MSOGI-QSG is experimentally shown to be a band-pass filter for the Figure 10 shows that the SOGI-FLL is immune to distorted grid voltage. Figure 9 demonstrates that the measured phase-angle is devoid of harmonic distortion and the 100Hz phase-angle frequency component.

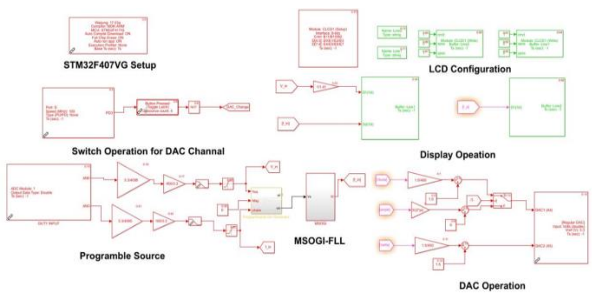


Figure 7. Model based programmingin STM32F407VG using waijung blockset of MATLAB/Simulink

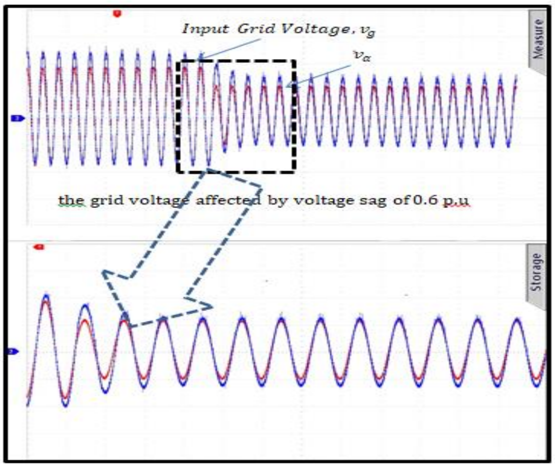
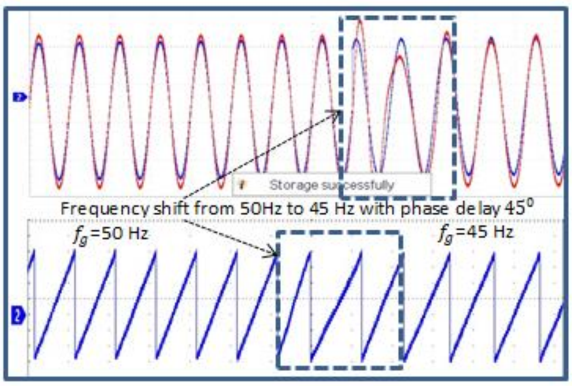


Figure 8. Experimental results of Test case:1. (Time Scale:20m-second/div; 0.5V/div)

MSOGI-FLL output signals, i.e. v_α/v_{in} and v_β/v_{in}, which are likewise devoid of harmonic distortion. Despite various irregularities affecting the grid voltage, the MSOGI-FLL continues to operate the same way. There is a single-phase voltage source converted, 10mH line inductor, auto-transformer and ARM cortex M4 microprocessor built as an experimental prototype for testing. The control algorithm was created in MATLAB/Simulink using the waijung blockset and then loaded onto a low-cost STM32F407VG ARM Cortex M4 microcontroller for general-purpose digital signal processing. Experimental results (see Figure 12) are carried out at 110V RMS grid voltage on experimental set-up (see Figure 11) at the point of common coupling. The sampling time of model base program is choosen 300micro-second. The control of single-phase grid tied inveter is developed using well-known synchronous reference frame current control techqnique.



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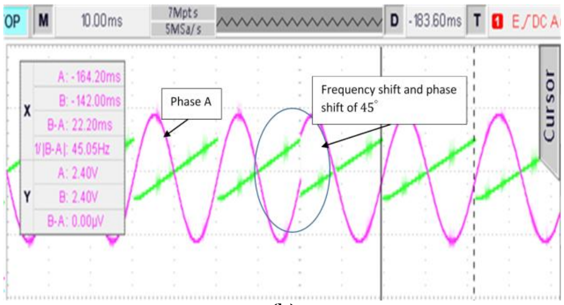

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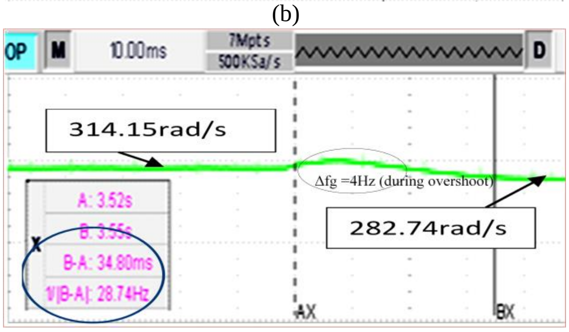

(c)

Figure 9. Experimental results of Test case:2. .(For (a)Time Scale:20m-second/div; 0.5V/div; (b) Time Scale:10m-second/div; 1V/div)

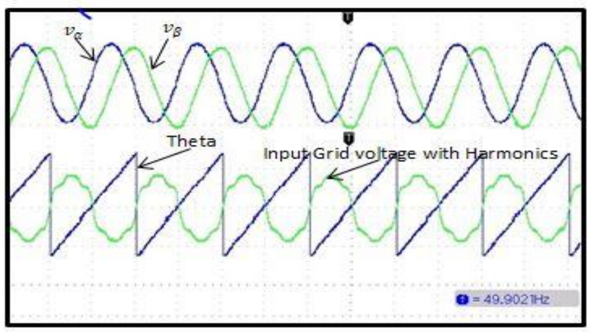

Figure 10. Experimental results of Test case:3.(Time Scale:10m-second/div; 1V/div)

Figure 11. Experimental setup of single-phase grid interfaced voltage source converter

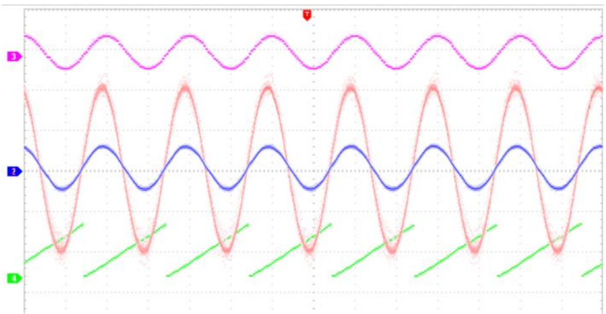

Figure 12. Experimental result of single-phase grid interfaced voltage source converter(Time scale:10ms//div) : (a)i_g(Pink and blue; Scale 4A/div), (b) i_g(Orage; Scale: 75V/div), and (c) theta (green)

5.DISCUSSION

Table 2 summarises the experimental findings for the single- phase grid voltage test scenarios.

It's possible to estimate the peak errors in the fundamental grid's parameters(e.g. amplitude, phase and frequency information), and tr stands for the settling time performance. The presented technique takes around 2.4 times as long to compute the grid's parameters as the current standard.

With the SOGI-OSG and DC signal cancellation block, MSOGI-FLL can achieve better immunity to DC-offset and harmonic noise. Both the SOGI–FLL and the SRF-PLL have frequency information that is impacted by the phase angle change. However, in the instance of the suggested method, the predicted frequency has a maximum overshoot of 4 Hz. With a net settling time of 34 ms, the suggested single-phase system has proven to have strong harmonics elimination and DC-offset rejection capabilities. There is therefore significant potential for the suggested system to identify harmonic and fundamental grid voltage characteristics selectively.

TABLE 2. Highlights of Comparative Performance Assessment

Cases	Peak Errors	SRF-PLL	SOGI-FLL	MSOGI-FLL
Voltage Drops	ΔA_g	-	-	-
	Δf_g	-	-	-
	$\Delta \theta_g$	-	-	-
	t_r	≈ 80	≈ 55	≈ 45
Freq.Step change	ΔA_g	≈ 2	-	-
	Δf_g(during oveshoot)	≈ 9	≈ 5	≈ 4
	$\Delta \theta_g$	$\approx 5^0$	$\approx 1.5^0$	$\approx 1.5^0$
	t_r	≈ 80	≈ 40	≈ 34
DC-Offset Elimination		NO	NO	YES
Harmonics Attenuation		NO	YES	YES
Steady-state Accuracy		Average	Good	Good
Control parameters		2	2	3
PI Tunning Required		YES	NO	NO

6. CONCLUSIONS

A good rejection of DC-offset, harmonics, and the frequency and phase-angle extraction may be achieved using MSOGI-FLL technique. Except for the existence of DC offset, SOGI-FLL can properly estimate the grid signal's frequency. Due to a DC offset in grid voltage, the predicted frequency has a 100Hz low frequency component. When harmonics are present, the distortion on this 100Hz ripple is amplified. The DG based inverter's synchronisation and control may be compromised as a result of this frequency estimate inaccuracy. Control parameter selection of SOGI-FLL is an art that balances the dynamic responsiveness, filtering capabilities, and required precision in detecting frequency and phase angle for single-phase grid-tied inverters under less than ideal grid circumstances.There is no ripple in the predicted synchronised frequency when using the Two essential blocks constitute the MSOGI-FLL structure: a basic SOGI-QSG architecture block modified with DC offset cancellation block, and a FLL for adaptively computing grid frequency.The dc offset cancellation block (i.e.third integrator) in MSOGI-FLL reduces the DC offset compared to the normal SOGI-FLL structure.Thus, the suggested technique is capable of rejecting DC offset and therefore correctly tracking the basic grid-voltage component frequency under all grid irregularities, in addition to the advantages of standard SOGI-FLL. In addition, the suggested systemis resistant to volatage sag/swell in the grid voltage and frequency fluctuations. Experiments results have shown that the proposed MSOGI-FLL seems to be more precise and has a superior transient stability than the conventional SOGI-FLL.

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Persian Abstract

چکیده

حلقه قفل فاز (PLL) در سیستم های متصل به شبکه برای همگام سازی عملکرد مبدل با ولتاژ شبکه اعمال می شود که بر پایداری و عملکرد مبدل تأثیر می گذارد. قاب مرجع سنکرون PLL (SRF-PLL) یک روش همگام سازی شبکه محبوب به دلیل سادگی و قابلیت اطمینان آن است. SRF-PLL معمولی نمی تواند آفست DC را سرکوب کند، که باعث نوسانات فرکانس و فاز اساسی می شود. وقتی یک شبکه نامنظم است، پهنای باند آن باید کاهش یابد تا از رد اختلال قابل قبول بدون کاهش سرعت تشخیص اطمینان حاصل شود. برای افزایش سرعت و دقت تخمین زاویه فاز، محققان ساختار را با افزودن فیلتر pre/in-loop در PLL های پیشرفته اصلاح کردند. ظرفیت ارائه پاسخ دینامیکی بهبود یافته و کاهش زمان ته نشینی بدون به خطر انداختن پایداری سیستم یا توانایی حذف اختلالات است. یک مشکل عمده برای PLL ها. در بین روش‌های کنترل مختلف، (SOGI-FLLحلقه قفل فرکانس مبتنی بر انتگرال‌گر تعمیم‌یافته مرتبه دوم) بهترین عملکرد را داشت. فرکانس ولتاژ شبکه را دقیقاً حتی زمانی که هارمونیک ها، تغییرات ولتاژ، نوسانات فرکانس و غیره وجود دارد، ردیابی می کند. در صورت افست DC، فرکانس محاسبه شده دارای نوسانات فرکانس پایین است. یک حلقه قفل فرکانس انتگرال‌گر تعمیم‌یافته مرتبه دوم (MSOGI-FLL)در این کار برای رسیدگی به ناهنجاری‌های ولتاژ شبکه از همه نوع، از جمله افست DC ارائه شده است. با استفاده از مجموعه بلاک Waijung از MATLAB/Simulink، یک SOGI-FLL اصلاح شده با اعمال موقعیت های ولتاژ شبکه غیرعادی با استفاده از یک میکروکنترلر STM32F407VGT مبتنی بر DSP کم هزینه تحقق و ارزیابی می شود. نتایج نشان‌دهنده عملکرد بهتر MSOGI FLL در شرایط سخت است.