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A Compact Model of Gate Capacitance in Ballistic Gate-all-around Carbon Nanotube Field Effect Transistors

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ABSTRACT

This paper presents a one-dimensional analytical model for calculating gate capacitance in Gate-All-Around Carbon Nanotube Field Effect Transistor (GAA-CNFET) using electrostatic approach. The proposed model is inspired by the fact that quantum capacitance appears for the Carbon Nanotube (CNT) which has a low density of states. The gate capacitance is a series combination of dielectric capacitance and quantum capacitance. The model so obtained depends on the density of states (DOS), surface potential of CNT, gate voltage and diameter of CNT. The quantum capacitance obtained using developed analytical model is 2.84 pF/cm for (19, 0) CNT, which is very close to the reported value 2.54 pF/cm. While, the gate capacitance comes out to be 24.3×10^{-2} pF/cm. Further, the effects of dielectric thickness and diameter of CNT on the gate capacitance are also analysed. It was found that as we reduce the thickness of dielectric layer, the gate capacitance increases very marginally which provides better gate control upon the channel. The close match between the calculated and simulated results confirms the validity of the proposed model.

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NOMENCLATURE

C	gate capacitance	**Greek Symbols**	
t_{ins}	thickness of insulator	ε_r	relative permittivity of gate dielectrical material
C_{cen}	centroid capacitance	ε_0	the permittivity of free space
C_q	quantum capacitance	ψ_s	surface potential (eV)
Q_{CNT}	linear charge density	V_{CNT}	surface voltage (V)
E_g	energy band gap	**Subscripts**	
U	fermi energy	s	source
$D_P(E)$	density of state at p^{th} subband	d	drain
		g	gate

1. INTRODUCTION

Due to scaling, the Complementary Metal-Oxide Semiconductor (CMOS) technology is facing lot of challenges which motivated researchers to look into different materials and structures for fabricating FET. Actually, the scaling of CMOS devices mainly degrades the performance of device due to increase in leakage current. This leakage current increases [1] further due to various short channel effects [2] including source/drain charge sharing, drain-induced barrier lowering (DIBL), subsurface punch through and velocity saturation. Due to limitations of MOSFET, conventional nano-scale SOI MOSFET which uses novel configuration gives better electrical performance but the complexity of these devices pushes the need to find out an alternative of FET devices [3]. In order to reduce these effects and enhance the device performance, carbon allotropes *i.e.* Carbon

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Nanotubes (CNTs) [4] are very promising material, due to their small size and remarkable electromechanical and thermal properties. Carbon nanotube field effect transistors (CNFETs) are better alternative to replace the Si-MOSFETs [5] due to better control of short channel effects, less propagation delay, high on-off current ratio and less power consumption [6-11] in nanometer (nm) dimension for the use in future computing system.

In CNFET devices, CNTs are channels between source and drain and the channel current through CNT is controlled by gate terminal. The CNFET has two geometrical structures: planar structure and Gate-All-Around (GAA) structure. The planar device performance is affected by fringing effect whereas the GAA structure is free from such effect due to its geometry hence, GAA structure is expected to be ideal geometry which maximizes the electrostatic gate control in FETs [12, 13].

Apart from various advantages, the major concern with CNFET is the effect of quantum capacitance on the performance of device. This is due to the fact that when the device has nanometer dimension, the quantum capacitance is comparable with electrostatic dielectric capacitance. In Si-MOSFET, it has been observed that quantum capacitance increases with increase in gate voltage [14]. The quantum capacitance is introduced in device when density of state (DOS) is very low or the energy level separation between states is very high [15]. So, it is important to investigate quantum capacitance of CNFET.

For CNFET, gate capacitance is a function of quantum capacitance and dielectric capacitance. The quantum capacitance for semiconducting single wall CNT (SWNT) (16, 8) has been already measured experimentally [16]. In past, various analytical models for gate capacitance have been proposed. Most of the proposed models are for planar structure only. Ahmed et al. [17] developed an analytical model for aligned CNT based FET with screening effects. This conformal mapping-based model is limited to the planar structure of CNFET. Singh [18] proposed an analytical expression for quantum capacitance. This analytical expression is based on the total charge density and analyzed that leakage current reduces for lower quantum capacitance but this expression is validated only for planar CNFET. Deyasi and Sarkar [19] developed a model for GAA-CNFET using Non-Equilibrium Green's Function (NEGF) method. They considered armchair (metallic) nanotube for CNFET but CNFET has semiconductor channel between source and drain. The novelty of the work lies in the choice the device structure with single CNT as channel which was further considered for modeling quantum capacitance for GAA-CNFET.

In this work, Gate-All-Around (GAA) structure is considered with single wall CNT as a channel. It has been assumed that conduction occurs in first sub-band and that there are no fringing effect and screening effect, due to

single wall CNT between source and drain and the structure is free from sharp edges.

This paper is organized in four sections. Section 2 describes the theory and model of quantum capacitance for channel (CNT). Section 3 explains the result and discussion obtained from analytical model and simulations and finally the conclusion of this study is given in section 4.

2. THEORY AND MODEL

Figure 1 shows the schematic view of GAA- CNFET considered for gate capacitance modeling. The gate capacitance (C_{total}) in CNFET is a series combination of dielectric capacitance (C_{ins}) and inversion layer capacitance (C_{inv}) which is given as follows:

$$C_{total} = \frac{C_{ins} \times C_{inv}}{C_{ins} + C_{inv}} \qquad (1)$$

where C_{ins} for gate-all-around structure is given by:

$$C_{ins} = \frac{2\pi\varepsilon_0\varepsilon_r}{ln\left(\frac{r_{CNT} + t_{ins}}{r_{CNT}}\right)} \qquad (2)$$

where ε_0 is the permittivity of free space, ε_r is the relative permittivity of gate dielectric material, r_{CNT} is the radius of CNT and t_{ins} is the dielectric thickness.

Further, the inversion layer capacitance (C_{inv}) is a series combination of centroid capacitance (C_{cen}) and quantum capacitance (C_q) [15]:

$$C_{inv} = \frac{C_{cen} \times C_q}{C_{cen} + C_q} \qquad (3)$$

C_{cen} can be ignored because we assume all changes to be located at the same position in the CNT layer. So:
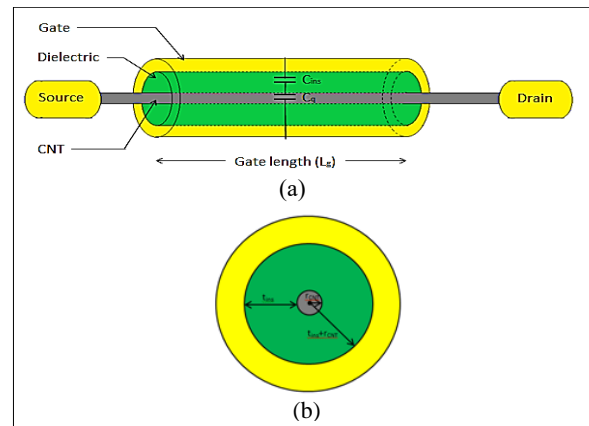

Figure 1. Schematic view of CNFET for modelling gate capacitance (a) front view (b) side view

$$C_{inv} = C_q \tag{3-a}$$

Equation (1) and (3-a), shows that the gate capacitance is a series combination of C_{ins} and C_q, which is given as:

$$C_{total} = \frac{C_{ins} \times C_q}{C_{ins} + C_q} \tag{4}$$

Quantum capacitance can be calculated by measuring the change in the linear charge density with surface potential [20].

$$C_q = \frac{d(\text{linear charge density})}{d(\text{surface potential})} = \frac{d(Q_{CNT})}{d(\psi_S)} \tag{5}$$

$$\psi_S = qV_{CNT} \tag{6}$$

so, Equation (5) can be rewritten as:

$$C_q = \frac{1}{q} \times \frac{d(Q_{CNT})}{d(V_{CNT})} \tag{7}$$

Linear charge density is the sum of charge density at source and drain terminals. The charge densities are different because V_{gs} and V_{ds} are independent and different. The total charge density (Q_{CNT}) on CNT surface is given as;

$$Q_{CNT} = Q_s + Q_d \tag{8}$$

where Q_s and Q_d are the charge densities at the source end and drain end of the channel, respectively.

Q_{CNT} is a function of Fermi-Dirac distribution and density of state (DOS). Hence, the total Q_{CNT} can be written as [21];

$$Q_{CNT} = \int_{E_C}^{\infty} \left[\left\{ \frac{D(E)}{2} F(E - U_s) \right\} + \left\{ \frac{D(E)}{2} F(E - U_d) \right\} \right] dE \tag{9}$$

D(E) is density of state which is a function of E, U_s and U_d are the fermi energy of source and drain, respectively.

There are n subbands, so the total charge for p^{th} subband is given as:

$$Q_P CNT = \int_{E_{CP}}^{\infty} \left[\begin{array}{c} \left\{ \frac{D_P(E)}{2} F(E - E_{CP} - U_s) \right\} + \\ \left\{ \frac{D_P(E)}{2} F(E - E_{CP} - U_d) \right\} \end{array} \right] dE \tag{10}$$

where E_{CP} is the conduction band minimum of pth subband. The conduction band minima is the difference of pth band energy (Δ_p) and surface potential (ψ_s) i.e:

$$E_{CP} = \Delta_P - qV_{CNT} \tag{11}$$

For one-dimensional structure, the general equation for density of state is given by [22]:

$$D(E) = \frac{D_0 E}{\sqrt{E^2 - \left(\frac{E_g}{2} \right)^2}} \tag{12}$$

where

$$D_0 = \frac{8}{3\pi V_\pi a_{c\text{-}c}} = 2 \times 10^9 \, m^{-1} eV^{-1}$$

$a_{c\text{-}c}$= Carbon-carbon length = 1.42 Å
$V\pi$= carbon-carbon bonding energy=3.0 eV
The DOS of pth subband is given by:

$$D_P(E) = \frac{D_0(E + \Delta_P)}{\sqrt{(E + \Delta_P)^2 - (\Delta_P)^2}} \tag{13}$$

Charge density at source is given by:

$$Q_s = \int_{E_{CP}}^{\infty} \frac{D_P(E)}{2} F(E - E_{CP} - U_s) \tag{14}$$

By using Equations (11) and (13), charge density of source becomes:

$$Q_s = \int_{E_{CP}}^{\infty} \left[\frac{D_0(E + \Delta_P)}{2\sqrt{(E + \Delta_P)^2 - (\Delta_P)^2}} \times \frac{1}{1 + exp\left(\frac{E - \Delta_P + qV_{CNT} - U_s}{kT} \right)} \right] dE \tag{15}$$

Similarly charge density at drain can be written as:

$$Q_d = \int_{E_{CP}}^{\infty} \frac{D_0(E + \Delta_P)}{2\sqrt{(E + \Delta_P)^2 - (\Delta_P)^2}} \times \frac{1}{1 + exp\left(\frac{E - \Delta_P + qV_{CNT} - U_d}{kT} \right)} dE \tag{16}$$

Equations (8), (15) and (16), give the total charge density:

$$Q_{CNT} = \int_{E_{CP}}^{\infty} \left[\frac{D_0(E + \Delta_P)}{2\sqrt{(E + \Delta_P)^2 - (\Delta_P)^2}} \times \left\{ \frac{1}{1 + e^{\left(\frac{E - \Delta_P + qV_{CNT} - U_s}{kT} \right)}} + \frac{1}{1 + e^{\left(\frac{E - \Delta_P + qV_{CNT} - U_d}{kT} \right)}} \right\} \right] dE \tag{17}$$

where; $U_s = qV_{gs}$; $U_d = qV_{ds}$

For SWCNT, as we considered 1st subband, so $\Delta_p = \Delta_1$ which is equal to the corresponding energy level minima (E) (i.e. Δ_1=E). So, from Equation (17):

$$Q_{CNT} = \frac{D_0}{2} \times \frac{2}{\sqrt{3}} \times \left[\frac{1}{1 + e^{\left(\frac{V_{CNT} - V_{gs}}{(V_T)} \right)}} + \frac{1}{1 + e^{\left(\frac{V_{CNT} - V_{ds}}{(V_T)} \right)}} \right] \tag{18}$$

In CNFET, two types of electric field exist: horizontal and vertical. Horizontal electric field is due to V_{ds}, which is responsible for the flow of current in the channel while the vertical electric field is due to V_{gs}, which is responsible to generate the charge carriers in channel. In this study for the calculation of total charge carriers on CNT, it was assumed that $V_{ds}=0$ and $V_{gs}=V_g$. So, Equation (18), can be written as follows:

$$Q_{CNT} = \frac{D_0}{\sqrt{3}} \times \left[\frac{1}{1+exp\left(\frac{V_{CNT}-V_g}{V_T}\right)} + \frac{1}{1+exp\left(\frac{V_{CNT}}{V_T}\right)} \right] \quad (19)$$

where, $(V_g - V_{CNT})$ can be calculated by [23]:

$$V_{g,CNT} = V_g - V_{CNT} = \begin{cases} 0 & for\ V_g < \Delta_1 \\ \alpha(V_g - \Delta_1) & for\ V_g > \Delta_1 \end{cases} \quad (20)$$

where α is slope of curve (V_g versus ψ_s), which is a function of device parameter, d (diameter of CNT).

From Equations (5) and (19), the quantum capacitance for SWCNT with first subband is as follows:

$$C_q = \frac{Q_{CNT}}{qV_{CNT}} = \frac{D_0}{\sqrt{3} \cdot qV_{CNT}} \times \left[\frac{1}{1+exp\left(\frac{V_{CNT}-V_g}{V_T}\right)} + \frac{1}{1+exp\left(\frac{V_{CNT}}{V_T}\right)} \right] \quad (21)$$

Quantum capacitance also depends on the chirality and diameter of CNT. As we increase the diameter of CNT, the energy bandgap and first sub-band minima also reduces and V_{CNT} increases.

3. RESULTS AND DISCUSSION

Quantum capacitance (C_q) is calculated using Equation (19) and further analyzed. In this study, CNT (19, 0) has been assumed for which the diameter is calculated using QuantumWise Atomistix Tool Kit (ATK) (QuantumATK O-2018.06) which comes out to be 1.49nm as illustrated in Figure 2. The thickness of dielectric layer and the channel length are considered as 8nm and 30nm, respectively which is feasible dimension for a practical GAA-CNFET [24]. The parameters considered for calculation used in Equation (19), are shown in Table 1.

In our previous work, it was demonstrated that La_2O_3 is the best gate dielectric material followed by HfO_2 and ZrO_2 [25, 26]. So, we used La_2O_3 ($\varepsilon_r =30$) as a dielectric layer in CNFET. The surface potential of CNT is calculated for different values of gate voltage (V_g). The value corresponding to 1.49nm diameter CNT for V_g and V_{CNT} are listed in Table 2 and $V_{g,CNT}$ calculated using Equation (20). For first sub-band energy minima of CNT, the value is calculated using simulation which comes out to be 0.281eV. Figure 3 shows the plot of quantum

Figure 2. Illustration of diameter calculation for (19, 0) CNT simulated using QuantumWise Atomistix Tool Kit (ATK)

TABLE 1. Parameters for quantum capacitance

S. No.	Parameters	Values
1.	CNT	Zigzag (19,0)
2.	Diameter of CNT	1.49nm
3.	Dielectric material	La_2O_3 (ε_r=30)
4.	Channel length	30nm
5.	Source to Drain Voltage (V_{ds})	0V

TABLE 2. Surface potential of CNT for different value of V_g [27]

V_g (volt)	V_{CNT} (volt)	$V_{g,CNT}$ (volt)
0	0	0
0.05	0.5	0
0.1	0.1	0
0.15	0.15	0
0.2	0.2	0
0.25	0.25	0
0.3	0.3	0
0.35	0.3276	0
0.4	0.3490	0.06305
0.45	0.3629	0.0871
0.5	0.3727	0.1261
0.55	0.3801	0.1699
0.6	0.3861	0.18915
0.65	0.3910	0.2590
0.7	0.3952	0.2522

capacitance (C_q) as a function of gate voltage. It is observed that initially C_q increases sharply with increase in V_g upto 0.4 Volt thereafter the slope of curve decreases

and peak is observed at $V_g = 0.5V$ and after that it gradually decreases with increase in V_g. The peak value of C_q obtained at V_g of 0.5V is 2.84pF/cm. The value obtained from this analytical work is compared with published results, which is listed in Table 3.

The gate capacitance of CNFET is calculated using Equation (1) for which C_{ins} is calculated with the help of Equation (2). By this analysis, the gate capacitance of CNFET comes out to be 24.3×10^{-2} pF/cm. In order to validate finding of this work, analytical work is compared with simulations [29]. Figure 4 shows the simulated results of gate capacitance versus gate voltage, which gives the C_{total} as 22.5×10^{-2} pF/cm at V_g of 0.5V.

Figure 5 shows the variation of gate capacitance with gate voltage for different dielectric layer thickness ($t_{ox} =$
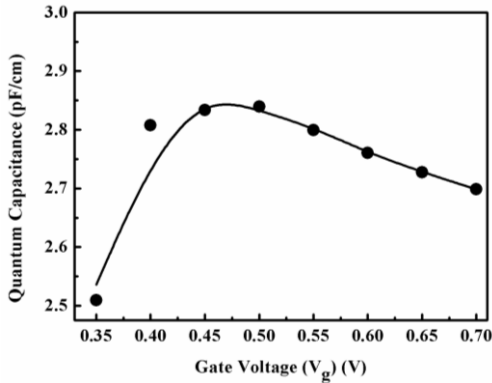
5nm, 7nm, 8nm and 9nm). This graph shows that as the dielectric thickness increases, gate capacitance decreases very marginally. This is inconsistent with the work presented by Deyasi and Sarkar [19], in which they have observed that quantum capacitance is not much affected by the thickness of dielectric layer. Table 4 shows the comparative analysis of analytical and simulated gate capacitance for the different thickness of dielectric layer. The close match between the two conform the validity of our proposed analytical model for gate capacitance of CNFET.

Figure 6 shows the variation of gate capacitance with gate voltage for different diameter of CNTs

Figure 3. Variation of quantum capacitance versus gate voltage for (19, 0) CNT

TABLE 3. Comparative analysis of quantum capacitance at $V_g = 0.5V$

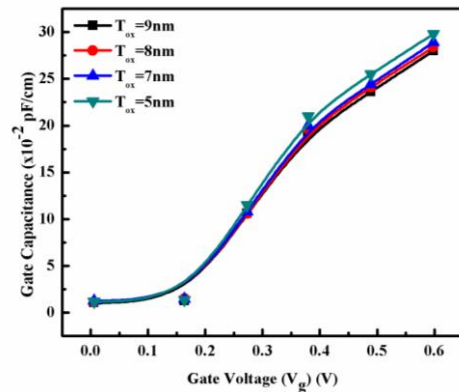| Research Group	Quantum capacitance (C_q) (pF/cm)
Mozahid and Ali [28]	3
Deyasi and Sarkar [19]	2.54
Proposed work	2.84
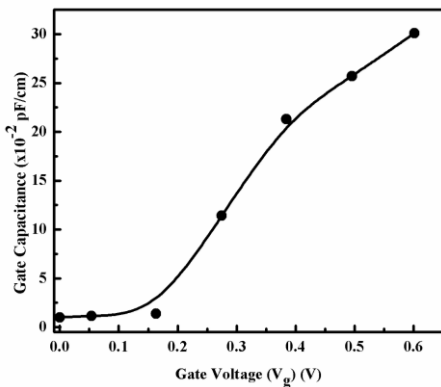
Figure 4. Simulation plot of gate capacitance versus gate voltage for CNFET

Figure 5. Simulation plot of gate capacitance versus gate voltage for CNFET with different gate dielectric thickness

TABLE 4. Comparison between analytical and simulated results for different thickness of dielectric layer

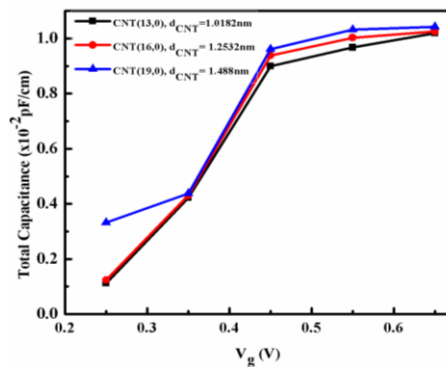| Thickness of dielectric layer (t_{ox})	Gate Capacitance ($\times 10^{-14}$ F/cm)	
	Analytical Work	**Simulated Work**
5nm	25.44	24.06
7nm	25.06	23.05
8nm	24.91	22.66
9nm	24.78	22.23

Figure 6. Simulation plot of gate capacitance versus gate voltage for CNFET with different diameter of CNT

(d$_{(13,0)}$=1.0182nm, d$_{(16,0)}$=1.2532nm and d$_{(19,0)}$=1.488nm). The total gate capacitance for CNT (19,0) is higher than CNT (13,0) and CNT (16,0) at V$_{gs}$ of 0.25V but it is increases marginally after V$_{gs}$ of 0.35V.

4. CONCLUSION

A new analytical model of gate capacitance for ballistic GAA-CNFET with SWCNT has been proposed and successfully investigated. To verify this model we used zigzag semiconductive CNT (19, 0) with the channel length of 30 nm. For La$_2$O$_3$ (ε_r=30) gate dielectric material, we obtained the quantum capacitance of 2.84 pF/cm and gate capacitance of 22.5×10^{-2} pF/cm at gate voltage of 0.5V. In order to verify the validity of proposed model, the results obtained were compared with experimental work available in literature. The close match between the calculated and experimental results confirms the validity of the proposed model. Further, the effect of gate dielectric thickness (5nm, 7nm, 8nm and 9nm) and diameter of CNT (1.0182nm, 1.2532nm and 1.488nm), on gate capacitance is also studied. It has been analysed that gate capacitance marginally decreases with increase in the thickness of gate dielectric layer, while increases with the rise in the diameter of CNT. Moreover, this model can be very well used to interpret the response of the CNFET towards variation of other dependent physical parameters. The results were compared with simulation results, and close match between the two, shows the validity of the proposed model for gate capacitance and also shows that the outcome of the performance of the device would remain consistent.

5. ACKNOWLEDGMENTS

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Persian Abstract

چکیده

در این مقاله یک مدل تحلیلی یک بعدی برای محاسبه ظرفیت گیت در ترانزیستور اثر میدان نانولوله کربن گیت (GAA-CNFET) با استفاده از روش الکترواستاتیک ارائه می شود. مدل پیشنهادی از این واقعیت الهام گرفته شده است که ظرفیت کوانتومی برای نانولوله کربنی (CNT)ظاهر می شود که دارای تراکم کم حالت است. ظرفیت گیت ترکیبی از ظرفیت دی الکتریک و ظرفیت کوانتومی است. مدل بدست آمده به چگالی حالتها (DOS) ، پتانسیل سطح CNT ، ولتاژ گیت و قطر CNT بستگی دارد. ظرفیت کوانتومی به دست آمده با استفاده از مدل تحلیلی توسعه یافته pF / cm ۲.۸۴ برای (۰/۰۱۹) CNT است که بسیار نزدیک به مقدار گزارش شده pF / cm ۲.۵۴ است. در حالی که ، ظرفیت گیت ۲۴.۳ × ۱۰-۲ pF / cm بیرون می آید. علاوه بر این، اثرات ضخامت و قطر دی الکتریک در ظرفیت گیت نیز مورد تجزیه و تحلیل قرار می گیرد. مشخص شد که هرچه ضخامت لایه دی الکتریک را کاهش می دهیم ، ظرفیت گیت بسیار کم افزایش می یابد که کنترل بهتر گیت روی کانال را فراهم می کند. تطابق نزدیک بین نتایج محاسبه شده و شبیه سازی شده ، اعتبار مدل پیشنهادی را تأیید می کند.