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Gain Boosted Folded Cascode Op-Amp with Capacitor Coupled Auxiliary Amplifiers

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ABSTRACT

A novel gain boosted folded cascode Op-Amp using simple single stage auxiliary amplifiers is presented. The proposed auxiliary amplifiers are designed in a way that has proper input and output DC common mode voltage without using common mode feedback network. The inputs of the auxiliary amplifiers are insulated by the coupling capacitors and floating-gate MOS transistors. Thus, the DC input voltage level limit has been removed. Diode connected transistors are also used in the output of the auxiliary amplifiers, which keep the output voltage level at the desired. A simple single stage auxiliary amplifier imposes fewer poles and zeroes on the main amplifier compared to more complicated amplifiers where consumes also less power consumption. Simulation results in a 0.18µm CMOS technology show a DC gain enhancement of about 20 dB while output swing, slew rate, settling time, phase margin, and gain-bandwidth retain almost as the same as previous folded cascode design.

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1. INTRODUCTION

One of the most popular approaches in designing high speed operational transconductance amplifiers (OTA) is the folded cascode (FC) architecture. Its popularity comes from high unity gain frequency, good output, and input swing. However, it has limitations to provide high DC gain which is required for some mixed-mode circuits like data converters. Active gain boosted folded cascode (GBFC) is presented first by Hosticka [1]. Through this technique, the output resistance and total gain can be increased by the gain of an auxiliary amplifier. This method increases the voltage gain without degrading its high-frequency performance. However, the GBFC introduces a pole-zero pair (doublet), which potentially leads to slow-settling behaviour of such op- amps [2,3,4].

The well-known active gain-boosting technique consists of the main amplifier and two auxiliary amplifiers is shown in Figure 1 [5]. By removing the auxiliary amplifiers and connecting the gate transistors of $M_{5\text{-}6}$ and $M_{7\text{-}8}$ to the appropriate bias voltages; a traditional folded cascode amplifier is shown in Figure 1. The auxiliary amplifiers should be operated at the specific input and output common mode voltages and therefore they usually utilize two individual common mode feedback networks [6].

There are also other methods presented in literatures that focus mostly on increasing the slew rate while their gain enhancement is not impressive [7-11]. Also, many applications like switched capacitor circuits demand a high gain one stage Op-Amp [12,13].

In this paper, a simple differential amplifier with positive feedback load has been utilized as an auxiliary amplifier. For this reason, the auxiliary amplifiers do not need their own common mode feedback circuit. As described later, coupling capacitors are used at the input of the auxiliary amplifiers so that there is no limit to the DC voltage range of the auxiliary amplifier input. Also, two different types of the auxiliary amplifiers with two different DC output voltage levels have been utilized for the purpose of providing proper output bias voltage.

2. PROPOSED AMPLIFIER

Figure 2 illustrates the equivalent half-circuit of the GBFC shown in previous figure. The body effect is ignored.

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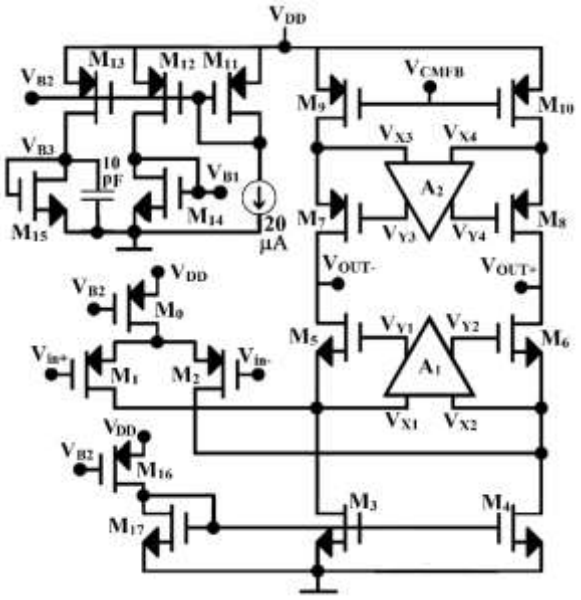

Figure 1. Conventional boosted-gain folded cascode

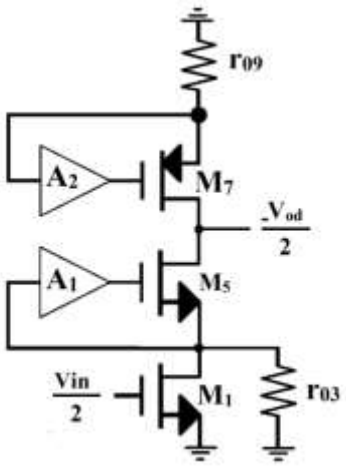

Figure 2. Equivalent half-circuit of the GBFC

Using KVL and KCL, the DC gain of the circuit can be written as:

$$\frac{v_{od}}{v_{in}} = -g_{m1}r_{o5}\frac{A_X^2 g_{m5}r_{o5}(r_{o1}\|r_{o3}) - 2A_X g_{m5}r_{o5}(r_{o1}\|r_{o3}) - 3A_X(r_{o1}\|r_{o3}) + g_{m5}r_{o5}(r_{o1}\|r_{o3}) + 3(r_{o1}\|r_{o3}) + 2(r_{o1}\|r_{o3})/g_{m5}r_{o5}}{\frac{3}{g_{m5}} + \frac{r_{o1}\|r_{o3}}{g_{m5}r_{o5}} + r_{o5} + r_{o1}\|r_{o3} - A_X r_{o5} - A_X(r_{o1}\|r_{o3})}$$

$$\cong g_{m1}r_{o5}\frac{A_X^2 g_{m5}r_{o5}(r_{o1}\|r_{o3})}{A_X r_{o5} + A_X(r_{o1}\|r_{o3})} \cong A_X g_{m1}\frac{r_{o5}(r_{o1}\|r_{o3})}{r_{o5}+(r_{o1}\|r_{o3})} \cong A_X g_{m1}(g_{m5}r_{o5}(r_{o1}\|r_{o3})\|g_{m5}r_{o5}r_{05}) = A_X g_{m1}(g_{m5}r_{o5}(r_{o1}\|r_{o3})\|g_{m7}r_{o7}r_{09}) = A_X A_{FC} \quad (1)$$

where the voltage gain of both auxiliary amplifiers, A_X, is almost assumed the same and relatively large. Also, $r_{o5} = r_{o7} = r_{o9}$ is considered. As can be seen, the voltage gain of the GBFC is approximately A_X times of FC.

The input DC voltage level of the first auxiliary amplifier A_1 (V_{X1} and V_{X2}) is about one overdrive voltage of M_4 & M_5 (V_{OV4}) and the output common mode voltage of A_1 should be around at $V_{GS5}+V_{OV4}$ for the output swing considerations. The proposed circuit of A_1 is illustrated in Figure 3a. As shown in this figure, gates of M_{1b} & M_{2b} isolated by coupling capacitors C_{1a} and C_{2a} from the main amplifiers, and the gate DC voltage level of M_{1b}-M_{2b} is supplied through quasi-floating gate transistors M_{7a} &M_{7b} which act as large resistors to V_{B3} [14].

The output common mode voltage of A_1 is stabilised by diode connected transistors M_{5a} & M_{6a} without using individual common mode feedback network at the DC voltage V_{G3a} which is proper for a driving gate of M_5 and M_6 transistors. The DC gain of A_1 can be obtained by:

$$A_X = gm_{1a}R_X \quad (2)$$

$$R_X = \left(gm_{5a}\text{-}gm_{3a}+gds_{5a}+gds_{3a}+gds_{1a}\right)^{-1} \quad (3)$$

while the value of gm_{3a} and gm_{3b} is approximately selected to 90 and 80 percent of gm_{5a} and gm_{5b}, respectively, to control the probable destructive effect of positive feedback [15]. In the same way, auxiliary amplifier A_2 has the same DC gain as A_1 and input coupling capacitors C_{1b} & C_{2b} as shown in Figure 3b. The output common mode voltage of A_2 is adjusted by diode connected M_{5b} & M_{6b} at dc level of V_{DD}-V_{SG5b} which is proper for biasing the gates of M_7 & M_8.

Boosting technique added a pole-zero doublet into the transfer function of GBFC. It can be shown that the zero location ω_Z is approximately equal to $(1+A_X)\omega_X$ where ω_X is the 3 dB cut-off frequency of auxiliary amplifiers and the zero is right close to its doublet pole [5, p.372]. The zero location ω_Z can be written as:

$$\omega_Z \approx A_X\omega_X \approx gm_{1a}R_X\frac{1}{R_X C_X} \approx \frac{gm_{1a}}{C_X} \quad (4)$$

where C_X donates the total load capacitance in the output of the auxiliary amplifier [16].

Hence, increasing the bias current of A_1 & A_2 has resulted in to greater gm_{1a}; therefore, higher value of zero location of ω_Z. The larger ratio of ω_Z to the unity frequency ω_U, the smaller the doublet effect [3]. Hence, with adjusting the tail current sources of A_1 & A_2 (Id9a & Id9b) slow settling caused by the doublet effect can be suppressed. The second pole location of the proposed auxiliary amplifier is far from its unity gain frequency and can be ignored. However, most of the reported GBFC amplifiers utilizing extra FC with a considerable

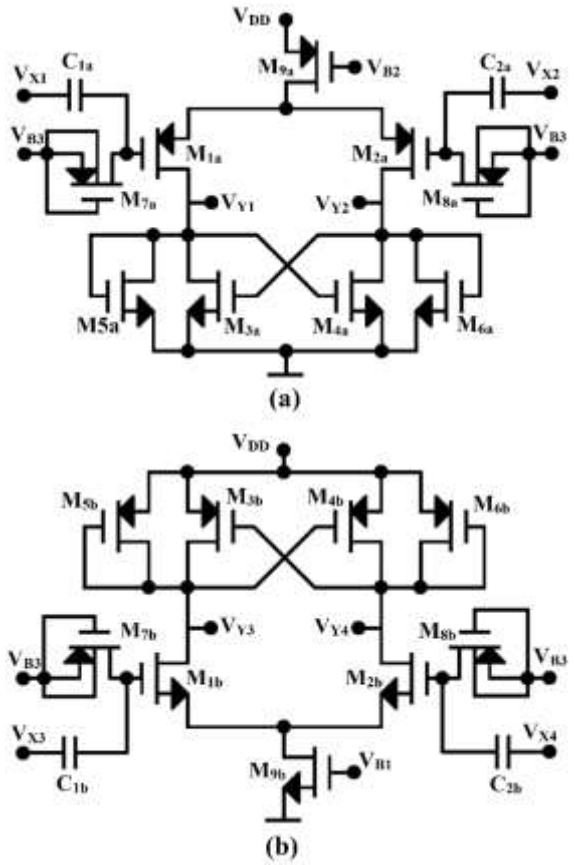

Figure 3. Proposed auxiliary amplifiers, A_1: (Figure 2a) and A_2: (Figure 2b)

TABLE 1. Transistor sizes(μm/μm) and component values

Transistor Number	W/L	Transistor Number	W/L
M_0	55/0.22	M_{1a}-M_{2a}	8/0.5
M_1-M_2	128/0.36	M_{3a}-M_{4a}	0.33/0.75
M_3-M_4	32/0.5	M_{5a}-M_{6a}	0.36/0.75
M_5-M_6	16/0.22	M_{7a}-M_{8a}	0.5/0.5
M_7-M_8	64/0.22	M_{9a}	6/0.22
M_9-M_{10}	32/0.22	M_{1b}-M_{2b}	4/0.5
M_{11}	5/0.22	M_{3b}-M_{4b}	0.8/0.5
M_{12}	0.5/0.22	M_{5b}-M_{6b}	1/0.5
M_{13}	1.25/0.18	M_{7b}-M_{8b}	0.5/0.5
M_{14}	0.5/0.22	M_{9b}	6/0.22
M_{15}	0.36/0.36	C_{1a}-C_{2a}	0.5pf
M_{16}	10/0.18	C_{1b}-C_{2b}	0.5pf
M_{17}	6.25/0.18		

secondary pole as an auxiliary amplifier which imposes a new pole to the main amplifier transfer function. Table 1 summarized the transistor sizes of the presented GBFC amplifier.

It should be noted that the amount of the C_{1a}, C_{2a}, C_{1b}, and C_{2b} should be large enough to ignore the parasitic capacitors located in the gate of transistors $M_{1a\text{-}2a}$ and $M_{1b\text{-}2b}$. For example, in Figure 3a, the effect of the parasitic capacitors located at the gates of M_{1a} and M_{2a} in differential mode small signal analysis can be written as:

$$v_{g1a} = \xi v_{X1};\ \xi = \frac{C_{1a}}{C_{1a} + C_{Par}},\ C_{Par} \cong C_{GS1a}. \quad (5)$$

In this paper, the value of C_{1a} is considered to 0.5 pF which be much larger than the C_{PAR}, so the ζ value is very close to one (about 0.98).

3. SIMULATION RESULTS

The two amplifiers were simulated in 0.18μm BSIM3v3 level 49 CMOS technology with 1.8 V of supply voltage by Hspice. The value of load capacitors C_{L1} & C_{L2} is 5 pF for both of the amplifiers. The frequency response of the amplifiers is shown in Figure 4 which shows DC gain enhancement of about 20 dB. A simple inverting amplifier with unity gain shown in Figure 5 is proposed for transient time simulation where C_1 = 1.5 pF and R_1 =

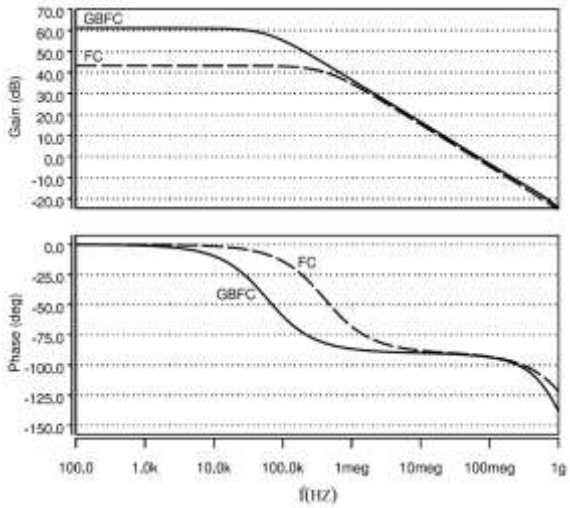

Figure 4. Open-loop frequency response of conventional FC and proposed GBFC amplifiers

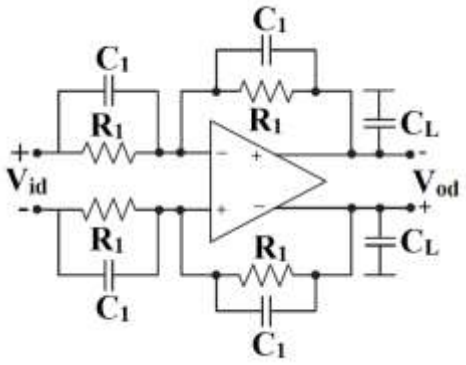

Figure 5. Inverting amplifier with unity gain

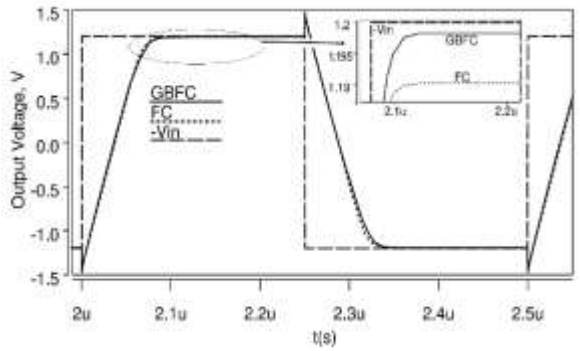

Figure 6. Step response of the amplifiers with 2.4 V_{P-P} of input

TABLE 2. Simulation results summary

Parameter	FC	GBFC
Power Supply	1.8	1.8
Power Dissipation	873	1018
DC Gain(dB)	42.2	61.9
1% Settling Time (nS)	76.8	83.4
Unity Gain Frequency(MHz)	58.5	54.1
Phase Margin(deg)	88.5	88.1
Diff. Output Swing(V)	2.4	2.4

5 MΩ. A square wave voltage with a range of ±1.2 V and a frequency of 2 MHz is applied to its differential input. The simulated differential outputs of the two circuits are shown in Figure 6. The simulation results summary is given in Table 2.

As can be seen, despite the increase in a voltage gain of the proposed amplifier, the maximum output swing of both amplifiers is the same. This is because the addition of auxiliary amplifiers has not caused any change in the DC operating point of the main transistors (M_0-M_{15}) in Figure 1.

To evaluate the effect of auxiliary amplifiers and validity of Equation (1), the frequency response of the auxiliary amplifiers is shown in Figure 7. As can be seen voltage gain of these amplifiers is about 22 dB which close to the enhancement gain of the GBFC over the FC.

Also, Table 3 presents the frequency characteristics of the proposed Op-Amp at different process corners. As can be seen, the GBFC has at least about 61.2 dB gain and 88.1° of phase margin at different process corners. Also, the value of the phase margin is considered under a capacitive load of 1pF and 10 pF which resulted in 76.7° and 88.9°, respectively.

The locations of the poles and zeros of the two amplifiers are shown in Table 4. It can be seen that the pole-zero doublets (-175 & -246 MHz) are large enough in comparison to the unity-gain frequency (ω_U) of the GBFC where ω_U is around 54 MHz. As illustrated by Ju and Lee [17], if the pole-zero doublet natural frequency is approximately four times the ω_U, their destructive effect on the step response can be ignored, which is almost the case here as well. It should be noted that the low-frequency pole and zeros below 1 Hz are omitted in Table 4.

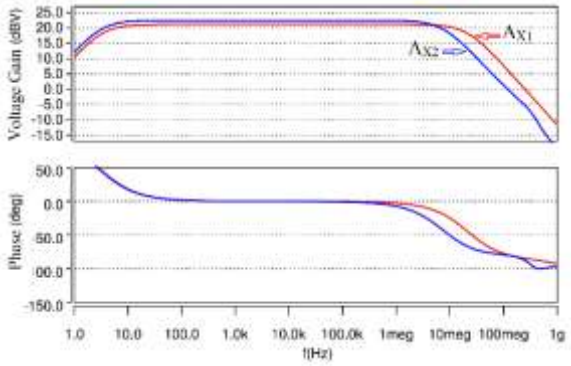

Figure 7. Frequency response of the Auxiliary amplifiers

TABLE 3. Proposed GBFC performance at different process corners with C_L=2×5pF

	TT	SS	SF	FS	FF
DC Gain(dB)	61.9	61.2	61.8	61.8	62.3
Unity Gain Frequency (MHz)	54.1	52	55.3	51.9	58.3
Phase Margin(deg)	88.1	88.1	88.2	88.3	88.3
Average 1% Sett. Time (nS)	83.4	118.5	108.3	98.2	81.9

TABLE 4. The location of poles and zeroes

	Poles (MHz)	Zeroes (MHz)
FC	-0.355	-6771
	-2280	
GBFC	-175.8324	-175.8270
	-246.7793	-246.6072
	-634.5±423.6i	-620.09
	-0.0402	

Figures 8 and 9 show Monte Carlo simulation results of 50 runs for the voltage gain and phase margin with a capacitive load of 5 pF, respectively. As shown in Figure 7, the mean (μ) and standard deviation (σ) of the DC voltage gain are 61.95 dB and 0.85 dB, respectively. Also, as can be seen in Figure 8, the mean and standard deviation of the phase margin are 87.74° and 0.26°, respectively. Monte Carlo simulation results show the GBFC is robust against process variations.

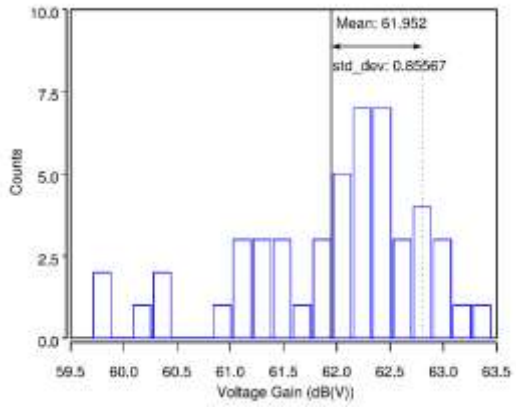

Figure 8. Monte Carlo simulation results for the voltage gain of the GBFC

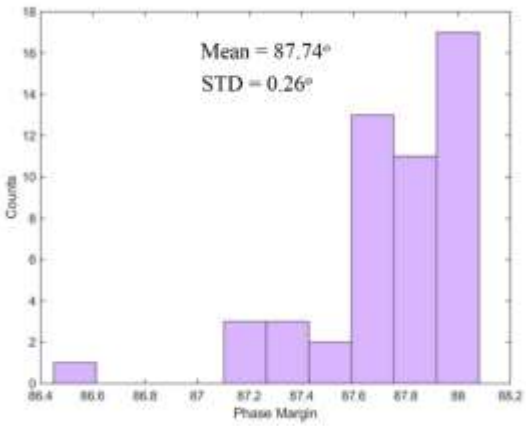

Figure 9. Monte Carlo simulation results for the phase margin of the GBFC

Note that both of the amplifiers have almost the same slew rate, unity gain frequency, phase margin, output swing range, and settling time while the proposed amplifier shows DC gain enhancement of about 20 dB. The power consumption of the GBFC is 1.02 mW while the FC amplifier consumes 0.87 mW, meaning the additional auxiliary amplifiers only consumed 0.145 mW or 14 percent of total power consumption.

4.CONCLUSION

Using two simple single stage amplifiers, the GBFC is presented. To achieve a proper swing at the output of the main amplifier, the input and output DC voltage levels of the auxiliary amplifiers must be set to certain values. The inputs of the auxiliary amplifiers are insulated by the coupling capacitors and therefore they can operate at any input DC voltage level. Diode connected transistors are also used in the output of the auxiliary amplifiers, which keep the output voltage level at the desired level without using an additional common mode feedback circuit. Simulation results show a DC gain enhancement of about 20dB without degrading the output swing and phase margin. The slow settling behaviour arising from the pole-zero doublet is also suppressed since the zero from the single stage auxiliary amplifier is shifted far from unity- gain frequency.

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Persian Abstract

چکیده

یک آپ امپ فولدد کسکود جدید با بهره افزوده شده و با استفاده از تقویت کننده های ساده کمکی ارائه شده است. تقویت کننده‌های کمکی پیشنهادی به گونه ای طراحی شده اند که دارای ولتاژ حالت مشترک ورودی و خروجی مناسب باشند. یک تقویت کننده کمکی یک طبقه ساده ، قطب ها و صفر های کمتری را به تقویت کننده اصلی تحمیل می کند، به علاوه در مقایسه با تقویت کننده های پیچیده تر مصرف توان کمتری نیز دارد. نتایج شبیه سازی با استفاده از فناوری 0.18µm CMOS نشان از افزایش بهره DC تقویت کننده در حدود ۲۰ دسی بل دارد. این در حالی است که سوئینگ مجاز در خروجی ، نرخ چرخش، زمان نشست، حاشیه فاز و پهنای باند تقویت کننده پیشنهادی تقریباً مشابه طراحی فولدد کاسکود مبنا است.