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Effect of Tail Capacitor on Phase Noise in LC Cross-connected Oscillators: An Analytical Investigation

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ABSTRACT

This paper investigates the effect of tail capacitance on phase noise of an LC-VCO (LC voltage-controlled-oscillator). First, the analytical relations of the phase noise for different values of tail capacitor (C_T) are derived and then for verifying them, simulation and calculated results are compared. For simplicity, three scenarios such as small, medium and large values of C_T are considered. In a case study an LC-VCO is designed in a standard 0.18μm CMOS technology, and simulation and numerical results have been presented for different values of C_T. In this case study, numerical analysis shows that for C_T =200fF (medium C_T) and C_T =10pF (large C_T), the phase noise at 1MHz offset from the 5.2GHz is -96dBc/Hz and -118dBc/Hz, respectively. According to the results, the ISF (Impulse sensitivity function) is improved by increasing the amount of C_T. Numerical values also demonstrate that excessive increase of C_T has no effect on the phase noise. While choosing bigger C_T can effectively reduce the noise contribution of the tail by bypassing the noise of tail transistor, but low impedance path generated by C_T may degrade the phase noise by reducing tank quality factor.

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1. INTRODUCTION

Oscillators are one of the important blocks in many applications such as RF electronics and digital systems. Since the oscillators have a non-linear behavior, it is very hard to model and analyze them. One of the most important parameters in oscillators is phase noise. The noise injected into the circuit by active and passive elements can show itself as a phase (frequency) perturbation in the desired signal which is called phase noise (or Jitter). Phase noise is one of the key parameters to determine the spectral purity of a signal generated by an oscillator. Depicted in Figure 1(a), single sideband (SSB) phase noise is defined as the ratio of the spectral power density measured at an offset frequency from the carrier (in 1Hz bandwidth) to the total power of the carrier signal and is stated as dBc/Hz. New communication circuits need low phase noise oscillators to satisfy the strict requirement of the modern communication standards. Among different type of oscillators [1], LC-VCOs attract many attentions due to their superior phase noise performance, reliable startup and ability for integration above standard CMOS technologies.

So far, several models for the prediction of phase noise were presented. Among these models, the most well-known phase noise model is Leeson's equation [2] in which the noise behavior of an oscillator is assumed linear-time-invariant (LTI). As reported in [2, 3] the verified Leeson's phase noise equation at offset frequency Δω from the oscillation frequency ω_0, is expressed as Equation (1).

$$L\{\Delta\omega\} = 10\times\log\left\{\frac{2FkT}{P_s}\times\left[\left(1+\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\times\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \tag{1}$$

in which k, T, P_s and Q_L are Boltzmann constant, absolute temperature, signal power and quality factor of the inductor respectively. $\Delta\omega_{1/f^3}$ is also the corner frequency and F denotes an experimental noise factor parameter. According to Figure 1(b) and (1), the plot can be divided into three regions. First region where $\Delta\omega >> \omega/2Q$ has a

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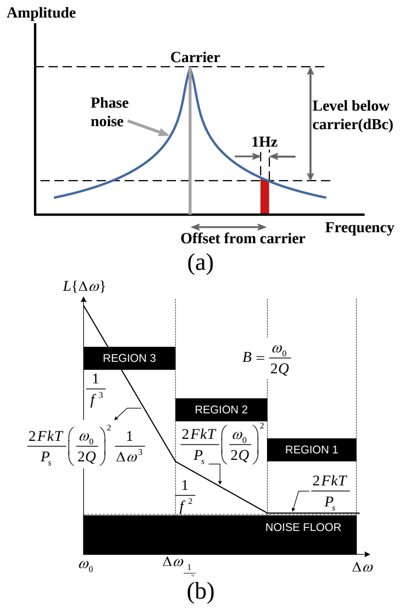


Figure 1. (a) Output spectrum of a practical oscillator and (b) different regions of phase noise vs frequency offset

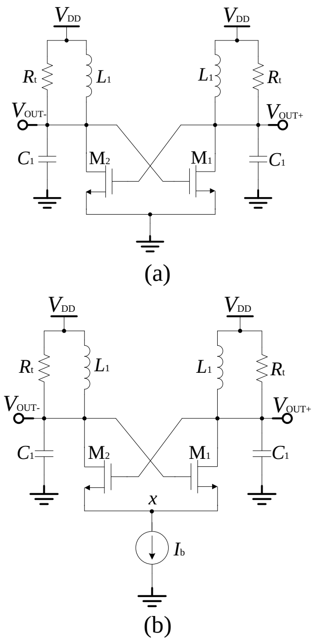


Figure 2. LC-tank oscillator (a) without current source and (b) with tail current source

flat profile and is dominated by the thermal noise. In regions two and three ($\Delta\omega << \omega / 2Q$) the white thermal noise and flicker noise make the phase noise with the slope of $1/\Delta\omega^2$ and $1/\Delta\omega^3$, respectively [4].

Alper Demir's model is one of the complex and accurate phase noise model (but almost without enough circuit intuition) [5]. In addition, the Demir's model can predict cyclostationary noise and also can present a fast simulation CADs [4].

As explained By Hajimiri et al. [3], in their phase noise model introduces a general theory of the phase noise for different kind of voltage-controlled oscillators (VCO) [4]. This model has a lower complexity with enough circuit intuition and can explain up and down conversion of noise in the close frequencies to the carrier. Another advantage of this model is that it introduces impulse-sensitivity-function (ISF) concept to consider the linear-time-variance (LTV) and cyclostationary behavior of noise in oscillators. The ISF is calculated by injecting an impulse current as the noise source of the device and measuring the phase shift (zero crossing) at the output voltage of the oscillator [6].

One of the oscillators which has the best performance in terms of phase noise amongst all CMOS VCOs is cross-connected LC-tank oscillator depicted in Figure 2 [3]. Figures 2(a) and 2(b) show two possible configurations of a cross-connected oscillator, i.e. without and with tail current source [7]. Using tail transistor is one of the ideas in the design of the cross-coupled LC-tank VCOs which was ignored in past decades. Later, it was considered more in [6, 8, 9] and discovered that it plays a prominent role in phase noise of the LC-tank VCO.

$$V_{OUT\pm} = \frac{4}{\pi} \times (R_t I_b) \tag{2}$$

While eliminating tail transistor in Figure 2(a) results in higher voltage headroom, using tail transistor in Figure 2(b) is preferred due to several reasons: first it creates a high impedance in series to the cross-connected switching transistors, reduces the loading of LC resonator and prohibits tank quality factor degradation [9]. Second, it defines the bias current I_b of the cross-connected pair and the output voltage of the oscillator as Equation (2) that results in more controllable and robust design against supply variations [6, 7, 10]. (R_t is loss of the LC-tank and I_b is the tail bias current.)

On the other hand, tail transistor can impose extra noise to the VCO and degrade the phase noise. Since the tail node (x) is a common mode node, the even harmonics especially second harmonic are usually dominant in that node. The switching cross-coupled pair, which acts as a single-balance mixer, up/down converts low frequency noise into two correlated sidebands around the fundamental frequency. It should be noted that the low-frequency noise in tail current source does not affect the phase noise directly. In fact, noise frequencies around the second harmonic is down converted close to the oscillation frequency [7, 10, 11]. It should be considered that because the level of the third and higher order harmonics is low and can be filtered by the LC-tank resonator, so the effect of the second order harmonic is dominant and significant in phase noise [6].

Filtering technique is one of the best options for eliminating the unwanted (second) harmonics caused by tail transistor and improving the phase noise of the oscillators [7]. Therefore, several techniques for attenuating the second harmonic in LC-tank oscillators have been proposed [7–9, 12–14], but the preferred technique is usually putting a capacitor in parallel to the tail transistor to bypass the second harmonic noise to ground. The tail capacitor acts as follows: (a) it attenuates the high-frequency noise components at tail node *x*, (b) prevents the up-conversion of the low-frequency noise of tail transistor into phase noise [9], and (c) reduces voltage variation at tail node and decreases the channel length modulation [9].

While using tail in Figure 2(b) produces a high impedance path, big shunt capacitor (C_T) bypasses it and results in loading the LC tank with lower impedance. In other words, LC tank is loaded through switching transistors by a low impedance and its quality factor is degraded. So, although a shunt capacitor to the tail node results in lower harmonic distortion in the output of the oscillator, it may degrade the quality factor of the LC-tank and accordingly the phase noise caused by switching transistors [6, 9]. In next section, we will conclude that the effect of harmonics filtering by C_T is more dominant than degradation of the quality factor on the phase noise.

It is worth mentioning as reported in literature [6, 9] the effect of capacitive noise filtering on phase noise is only investigated by simulation but no analysis is presented. Further, Andreani et al. [15] used a closed-form symbolic formula for phase noise of cross-connected oscillators in the case of negligible C_T is obtained by using phase noise relation in (3) which was introduced by Hajimiri [6] and others [15].

$$L\{\Delta\omega\} = 10 \times \log_{10}(\sum \frac{\Gamma^2{}_{rms} \times \overline{i_n^2} / \Delta f}{2 \times q^2{}_{\max} \times \Delta\omega^2}) \tag{3}$$

where $\overline{i_n^2} / \Delta f$ and $\Gamma_{\rm rms}$ represent the power spectral density of the current noise source and the root-mean-square of the ISF respectively. The maximum charge at output capacitor is denoted by q_{max}. By neglecting C_T (i.e. very small tail capacitances), a phase noise closed-formula obtained from literature [6, 15] as follows:

$$L(\Delta\omega) = 10 \times \log[\frac{k_B T}{N^2 C^2 A^2 \Delta\omega^2 R_t} \times (\gamma + 1 + \frac{\eta[\Phi]}{N} \gamma g_m R_t)] \tag{4}$$

in which K_B, g_m, A and C are, respectively, the Boltzmann constant, the transconductance of each transistor, the amplitude of output voltage and total capacitance of LC tank. $\eta[\Phi]$ represents the tail current phase noise coefficient [16], N=1 for single-ended and N=2 for differential oscillators. Apparently, C_T and its effect are not presented in (4).

Recently, Razavi [16] has been presented an intuitive but very instructive discussion for the effect of tail capacitance on oscillator phase noise. It was explained that the tail capacitance bypasses the second harmonics of tail node, produces a doublet around each zero-crossing, results in up-conversion of flicker noise of cross-connected transistors and also shunts the noise of tail transistor (at $2\omega_0$) to ground.

On the other hand, along with different phase noise analyses, several researches were also devoted to the phase noise reduction of LC oscillators and different techniques have been introduced in literature. Since zero crossing points are strongly vulnerable to the noise, in literature [17] a phase noise reduction technique is presented by pushing high closed-loop gain to the non-zero-crossing points of the outputs. In order to reduce the close-in phase noise caused by the flicker noise of tail transistor, a resistive feedback is used in literature [18] and the flicker noise of the tail transistor has been suppressed. However, such a diode-connected tail transistor reduces the output impedance of tail and may degrade the quality factor of the tank. Current-switching as well as capacitive-degeneration techniques are utilized simultaneously to reduce the flicker and thermal noise of tail and cross-connected transistors [19].

In this paper the effect of different values of tail capacitor on total phase noise is analytically studied and compared with simulation results. The rest of the paper is organized as follows: the phase noise analysis in a cross-connected VCO for three scenarios of C_T are described in Section 2 and a closed-formula for each ISF is presented. Section 3 compares simulation results with numerical values obtained by derivations. Finally, conclusions are given in Section 4.

2. PHASE NOISE ANALYSIS FOR SMALL, MEDIUM AND LARGE VALUES OF TAIL CAPACITANCES

In the LC-tank oscillator shown in Figure 3(a), the differential cross-connected transistors make a negative transconductance that can eliminate the loss of the LC tank [6, 8, 9]. For an LC-tank oscillator with arbitrary phase of sinusoidal output, the output voltage can be described by Equation (5):

$$\begin{aligned} V_{OUT+}(\varphi) &= A_{TANK} \times \sin(\varphi) \\ V_{OUT-}(\varphi) &= -A_{TANK} \times \sin(\varphi) \end{aligned} \tag{5}$$

Denoting DC bias current of tail transistor by $2I_B$, the current of M_1 and M_2, and the total current of them can be written as Equations (6), (7) and (8), respectively.

$$I_1(\varphi) = \frac{\beta}{2}(A_{TANK} \times \sin(\varphi) + V_S(\varphi))^2 \tag{6}$$

$$I_2(\varphi) = \frac{\beta}{2}(-A_{TANK} \times \sin(\varphi) + V_S(\varphi))^2 \tag{7}$$

$$2I_B = I_1(\varphi) + I_2(\varphi) \tag{8}$$

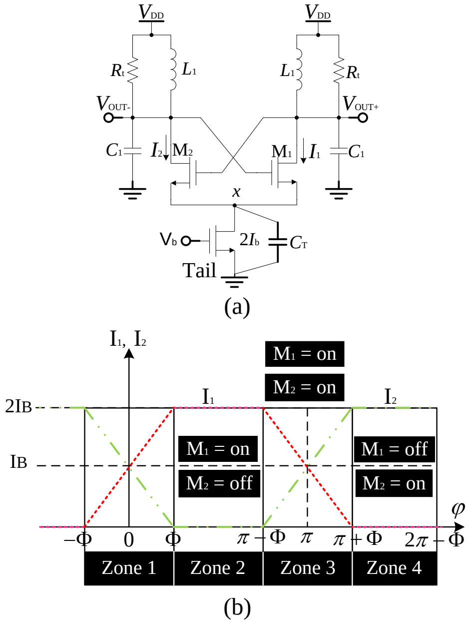


Figure 3. (a) Cross-connected LC-tank oscillator with C_T, and (b) ideal current of transistor versus φ

where $\beta = \mu C_{ox}\dfrac{w}{l}$, and $V_S(\varphi)$ is given by Equation (9).

$$V_S(\varphi) = \sqrt{\frac{2I_B}{\beta} - A^2_{\mathrm{Tank}}\sin^2(\varphi)} \tag{9}$$

The current of each cross-connected transistor (i.e. I_1 and I_2) is depicted in Figure 3(b) for one period in which 2Φ is the conduction angle. By substituting Equation (9) into Equation (7) and setting the equation to zero, the half conduction angle Φ is obtained as Equation (10).

$$\Phi = \arcsin\sqrt{\frac{I_B}{\beta \times A^2_{TANK}}} \tag{10}$$

Considering (6), (7) and (9), the transconductance of M_1 and M_2 can be given by Equations (11) and (12).

$$g_{m1}(\varphi) = \beta A(\sin(\varphi) + \sqrt{2\sin^2(\Phi) - \sin^2(\varphi)}) \tag{11}$$

$$g_{m2}(\varphi) = \beta A(-\sin(\varphi) + \sqrt{2\sin^2(\Phi) - \sin^2(\varphi)}) \tag{12}$$

According to Figure 3(b) the cross-connected transistors operate in four different zones during each period. Due to switching of M_1 and M_2 the current of each transistor is usually supposed as a square waveform shown in Figure 3(b) (though the LC tank operates as a narrowband filter and generates sinusoidal output voltages). As discussed earlier, in order to reduce the noise of tail transistor, a capacitor C_T is placed between node x and ground. In this section, we will discuss about the effect of tail capacitive filtering by derivation of the ISF for three scenarios of C_T, *i.e. very small, medium and big* C_T.

The ISF of tank resistance R_t at nodes V_{OUT+} and V_{OUT-} (denoted by $\Gamma_{Rt,+}$, $\Gamma_{Rt,-}$) is independent of tail capacitance and has been derived Andreani and Wang [20] as Equation (13).

$$\Gamma_{Rt,+}(\varphi) = \frac{\cos(\varphi)}{N} \quad , \quad \Gamma_{Rt,-}(\varphi) = -\frac{\cos(\varphi)}{N} \tag{13}$$

2.1. Derivation of ISF When CT Is Medium

In prior works, the ISF of oscillator has been calculated with the assumption of negligible C_T. In the case of non-negligible C_T, the charge of C_T cannot be discharged completely during each period. In order to model it, we define a factor α as the ratio of discharged ΔQ_d to the total charge ΔQ of C_T. The amount of charge for C_T during a period (while discharging through transistors $M_{1,2}$) is obtained by Equation (14).

$$Q_{C_T}(t) = \Delta Q \times e^{-\frac{t}{\tau}} \tag{14}$$

where τ is the time constant of tail node x ($\tau = C_T/g_{m1,2}$). The charge variation (ΔQ_d) of node x can be calculated by Equation (15).

$$\Delta Q_d = \Delta Q - Q_{C_T} = \Delta Q(1 - e^{-\frac{t}{\tau}}) \tag{15}$$

So, the factor α is obtained as follows:

$$\alpha = \frac{\Delta Q_d}{\Delta Q} = (1 - e^{-\frac{t}{\tau}}) \tag{16}$$

2. 1. 1. Calculation of Γ_{ids}

2. 1. 1. 1. Zone 2 ($\Phi < \varphi < \pi - \Phi$) In this zone M_1 is on and M_2 is off. As shown in Figure 4(a), applying $\overline{i^2_{ds1,n}}$ as an impulse current of area ΔQ charges C_1 and C_T by ΔQ and $-\Delta Q$, respectively. If we assume that C_T is not so small, the time constant of node x is comparable with period of oscillation and as a result C_T is not fully discharged as shown in Figure 4(a). If only $\Delta Q_d = -\alpha.\Delta Q$ is transferred from C_T to C_1 in each period, the final charge of C_1 and voltage variation at output node are as Equations (17) and (18), respectively.

$$\Delta Q_1 = \Delta Q - \alpha.\Delta Q = (1-\alpha)\Delta Q \tag{17}$$

$$\Delta V_1 = (1-\alpha)\Delta V \tag{18}$$

Also, the charge and voltage variation of C_T (i.e. tail node) can be express as Equations (19) and (20), respectively.

$$\Delta Q_T = -(1-\alpha)\Delta Q \tag{19}$$

$$\Delta V_T' = (\alpha - 1)\Delta V_T \tag{20}$$

whrere,

$$\Delta V_T = \frac{C_1}{C_T}\Delta V_1 \tag{21}$$

As seen in Equations (20) and (21), contrary to the case with negligible C_T, in this case the voltage of C_T is non-zero and can affect tank voltage through M_1 (as a common-gate configuration with gain A_{CG}). Since the voltage at C_T is amplified by $A_{CG}=g_{m1}R_t$, the total voltage change at output node is obtained as Equation (22).

$$\Delta V_1' = \Delta V_1 + A_{CG,1}\times\Delta V_T' \tag{22}$$

By substituting Equations (18), (20) and (21) into Equation (22), we have:

$$\begin{aligned}\Delta V_1' &= (1-\alpha)\Delta V + A_{CG,1}(\alpha-1)\times\frac{C_1}{C_T}\Delta V\\ &= \Delta V_1' = (1-g_{m1}.R_T\frac{C_1}{C_T})\times(1-\alpha)\Delta V\end{aligned} \tag{23}$$

As known from [16], ΔV results in $\Gamma_{Rt}=\frac{\cos(\varphi)}{N}$ and thus according Equation (23) in this zone $\Gamma_{ids,1}$ can be obtained as Equation (24).

$$\Gamma_{i_{ds1}} = (1-g_{m1}R_t\frac{C_1}{C_T})(1-\alpha)\Gamma_{Rt} \tag{24}$$

2. 1. 1. 2. Zones 1 and 3 ($-\Phi<\varphi<\Phi$, $\pi-\Phi<\varphi<\pi+\Phi$)

Since M_1 and M_2 are simultaneously on in this zones, the charge of $-\alpha.\Delta Q$ this time is passed from C_T through both of the transistors to capacitors C_1 and C_2, as depicted in Figure 4(b). The final charge and voltage variation of C_1 are obtained by Equations (25) and (26), respectively.

$$\Delta Q_1 = \Delta Q - \frac{g_{m1}}{g_{m1}+g_{m2}}\times\alpha\Delta Q = \frac{g_{m2}+(1-\alpha)g_{m1}}{g_{m1}+g_{m2}}\Delta Q \tag{25}$$

$$\Delta V_1 = \frac{g_{m2}+(1-\alpha)g_{m1}}{g_{m1}+g_{m2}}\Delta V \tag{26}$$

Also, the final charge and voltage variation of C_2 are given as follows:

$$\Delta Q_2 = \frac{-\alpha\times g_{m1}}{g_{m1}+g_{m2}}\Delta Q \tag{27}$$

$$\Delta V_2 = \frac{-\alpha\times g_{m2}}{g_{m1}+g_{m2}}\Delta V \tag{28}$$

Again, considering the effect of none-zero voltage of C_T on C_1 and C_2 and fully correlation of ΔV_1 with ΔV_2 [15], total voltage change at C_1 (i.e.$\Delta V_1'$) is expressed by Equation (29).

$$\begin{aligned}\Delta V_1' = \Delta V_1 &+ A_{CG,1}(1-\alpha)\times\Delta V_T -\\ &\to \Delta V_2 - A_{CG,2}(1-\alpha)\Delta V_T\end{aligned} \tag{29}$$

By replacing Equation (21), (26) and (28) in Equation (29) we have Equation (30).

$$\begin{aligned}\Delta V_1' = &\frac{g_{m2}+(1-\alpha)g_{m1}}{g_{m1}+g_{m2}}\Delta V + (g_{m1}.R_T\frac{C_1}{C_T})(\alpha-1)\Delta V -\\ &\to \frac{\alpha\times g_{m2}}{g_{m1}+g_{m2}}\Delta V - (g_{m2}.R_T\frac{C_1}{C_T})(\alpha-1)\Delta V\end{aligned} \tag{30}$$

Simplifying Equation (30), Equation (31) is obtained.

$$\begin{aligned}\Delta V_1' = &[(g_{m1}-g_{m2})(\alpha-1)R_T\frac{C_1}{C_T}+\\ &\to \frac{(1+\alpha)\times g_{m2}+(1-\alpha)\times g_{m1}}{g_{m1}+g_{m2}}]\Delta V\end{aligned} \tag{31}$$

Finally, one can obtain $\Gamma_{i_{ds1}}$ as Equation (32).

$$\begin{aligned}\Gamma_{i_{ds}1}(\varphi) = &[(g_{m1}-g_{m2})(\alpha-1)R_T\frac{C_1}{C_T}+\\ &\to \frac{(1+\alpha)\times g_{m2}+(1-\alpha)\times g_{m1}}{g_{m1}+g_{m2}}]\times\Gamma_{Rt}\end{aligned} \tag{32}$$

2. 1. 1. 3. Zone 4 ($\pi+\Phi<\varphi<2\pi-\Phi$)

Apparently, in this zone M_1 is off and does not contribute to the phase noise of output voltage. So, we have: $\Gamma_{ids1}(\varphi)=0$. Accordingly, the impulse sensitivity function of M_1 during a period is summarized as follows:

$$\Gamma_{i_{ds}}(\varphi) = \begin{cases} [(g_{m1}-g_{m2})(\alpha-1)R_T\frac{C_1}{C_T}+ \\ \to \frac{(1+\alpha)\times g_{m2}+(1-\alpha)\times g_{m1}}{g_{m1}+g_{m2}}]\times\Gamma_{Rt}(\varphi) & -\Phi<\varphi<\Phi \\ (1-g_{m1}R_t\frac{C_1}{C_T})(1-\alpha)\Gamma_{Rt} & \Phi<\varphi<\pi-\Phi \\ [(g_{m1}-g_{m2})(\alpha-1)R_T\frac{C_1}{C_T}+ \\ \to \frac{(1+\alpha)\times g_{m2}+(1-\alpha)\times g_{m1}}{g_{m1}+g_{m2}}]\times\Gamma_{Rt}(\varphi) & \pi-\Phi<\varphi<\pi+\Phi \\ 0 & \pi+\Phi<\varphi<2\pi-\Phi \end{cases} \tag{33}$$

It is worth mentioning that the channel current noise of M_1 and M_2 is a cyclostationary noise and can be written as Equation (34).

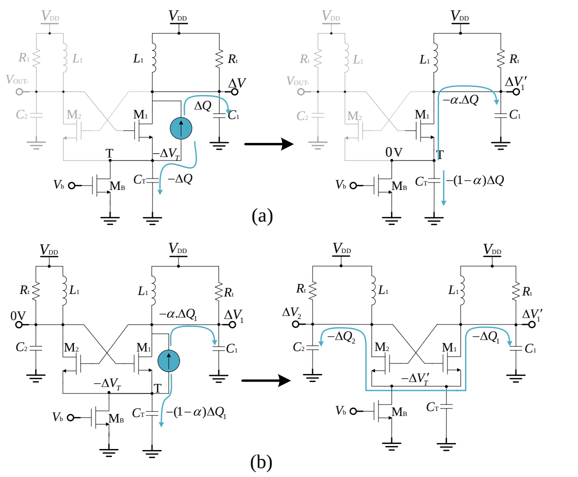


Figure 4. ISF derivation when C_T is not small, (a) only M_1 is on and (b) both transistors are on

$$\overline{i_n^2(t)} = \overline{i_n^2} \times \sigma(t)\,, \tag{34}$$

where $\overline{i_n^2}$ is a stationary term and $\sigma(t)$ is the noise modulation factor (NMF) which can be derived easily from noise characteristic relation [3]. According to Andreani et al. [15] and using $g_{m1}(\varphi)$ in Equation (11), the channel thermal noise of M_1 can be written as (35). Comparing Equation (35) with Equation (34), the NMF is easily obtained as Equation (36).

$$\begin{aligned} &\overline{i_n^2}(t) = 4KT\gamma g_{m1}(\varphi) = \\ &\rightarrow 4KT\gamma\beta A_{\tan k} \times (\sin(\varphi) + \sqrt{2\sin^2(\Phi) - \sin^2(\varphi)}) \end{aligned} \tag{35}$$

$$\sigma(t) = \sqrt{(\sin(\varphi) + \sqrt{2\sin^2(\Phi) - \sin^2(\varphi)})} \tag{36}$$

Based on Hajimiri's theorem, in the case of cyclostationary noise, effective root mean square (RMS) of ISF (i.e. $\Gamma_{ids,eff}$) should be calculated from Equation (33). Since the integral equation of $\Gamma_{ids,eff}$ has no algebraic closed-form expression, the closed-form symbolic formulas for RMS value of Equation (33) is not presented here. Instead, using numerical methods the numerical values of $\Gamma_{ids,eff}$ for required Φ are presented in the next section.

2. 1. 2. Derivation of Tail ISF (Γ_{Tail}) As depicted in Figure 5, the impulse current noise of $\overline{i_{n,tail}^2}$ charges C_T with charge area of ΔQ. It should be noted that impulse current only passes through C_T and does not charge $C_{1,2}$.

2. 1. 2. 1. Zones 1 and 3 In these zones both of the transistors are on and $\alpha \times \Delta Q$ from C_T is discharged through M_1 and M_2 to the output capacitors (C_1, C_2) that results in charge variation of ΔQ_1 and ΔQ_2 respectively.

As similar to previous section one can calculate the charge and voltage variation at outputs ($C_{1,2}$) by Equation (37) to Equation (40).

$$\Delta Q_1 = \frac{g_{m1}}{g_{m1} + g_{m2}} \times \alpha\Delta Q \tag{37}$$

$$\Delta Q_2 = \frac{g_{m2}}{g_{m1} + g_{m2}} \times \alpha\Delta Q \tag{38}$$

$$\Delta V_1 = \frac{g_{m1}}{g_{m1} + g_{m2}} \times \alpha\Delta V \tag{39}$$

$$\Delta V_2 = \frac{g_{m2}}{g_{m1} + g_{m2}} \times \alpha\Delta V \tag{40}$$

Once again, considering the correlation between outputs and effect of residual charge of C_T, the total voltage variation due to $\overline{i_{n,tail}^2}$ at capacitor C_1 can be written as:

$$\begin{aligned} &\Delta V_1' = \Delta V_1 + A_{CG,1}(1-\alpha)\Delta V_T - \Delta V_2 - \\ &\rightarrow A_{CG,2}(1-\alpha)\Delta V_T \end{aligned} \tag{41}$$

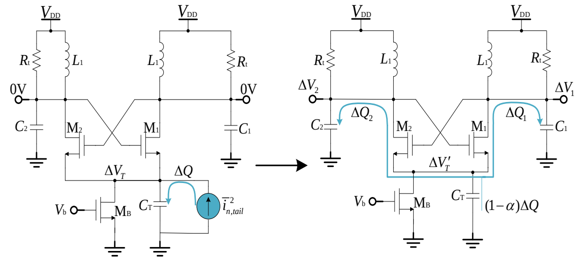


Figure 5. Circuit for calculating ISF of tail noise when C_T is not small in zones 1 and 3

Using Equations (39), (40) and (21), Equation(41) is rewritten as follows:

$$\begin{aligned} &\Delta V_1' = \frac{g_{m1}}{g_{m1} + g_{m2}} \times \alpha\Delta V + g_{m1}R_T\frac{C_1}{C_T}(1-\alpha)\Delta V - \\ &\rightarrow \frac{g_{m2} \times \alpha\Delta V}{g_{m1} + g_{m2}} - g_{m2}R_T\frac{C_1}{C_T}(1-\alpha)\Delta V \end{aligned} \tag{42}$$

As a result, the impulse sensitivity function of tail can be derived as follow:

$$\begin{aligned} &\Gamma_{Tail}(\varphi) = (g_{m1} - g_{m2})[\frac{\alpha}{g_{m1} + g_{m2}} + \\ &\rightarrow R_T\frac{C_1}{C_T}(1-\alpha)] \times \Gamma_{Rt}(\varphi) \end{aligned} \tag{43}$$

2. 1. 2. 2. Zone 2 In this zone M_1 is on and M_2 is off and similar to previous section $\alpha \times \Delta Q$ from C_T is discharged to C_1 and total voltage change of output voltage can be express as bellow.

$$\begin{aligned} \Delta V_1' &= \Delta V_1 + A_{CG,1}(1-\alpha)\Delta V_T \\ &= [\alpha + g_{m1}R_t(1-\alpha)\frac{C_1}{C_T}]\Delta V \end{aligned} \tag{44}$$

So, the ISF of tail in this zone is given by Equation (45).

$$\Gamma_{Tail}(\varphi) = [\alpha + g_{m1}R_t(1-\alpha)\frac{C_1}{C_T}] \times \Gamma_{Rt}(\varphi) \tag{45}$$

2. 1. 2. 3. Zone 4 In this zone M_2 is on and M_1 is off, charge $\alpha \times \Delta Q$ is transferred to C_2 and results in $\alpha \times \Delta V$. Considering the residual charge on C_T, total voltage variation at C_2 is given by $\Delta V_2 = [\alpha + g_{m2}R_t(1-\alpha)\frac{C_1}{C_T}]\Delta V$. Again, with regard to the fully correlation of differential outputs, $\Delta V_1 = -\Delta V_2$ and accordingly ISF is obtained. So, the ISF of the tail in a period is given by Equation (46):

$$\Gamma_{Tail}(\varphi) = \left\{ \begin{array}{ll} (g_{m1} - g_{m2})[\frac{\alpha}{g_{m1} + g_{m2}} + R_T\frac{C_1}{C_T}(1-\alpha)] \times \Gamma_{Rt}(\varphi) & -\Phi < \varphi < \Phi \\ [\alpha + g_{m1}R_t(1-\alpha)\frac{C_1}{C_T}] \times \Gamma_{Rt}(\varphi) & \Phi < \varphi < \pi - \Phi \\ (g_{m1} - g_{m2})[\frac{\alpha}{g_{m1} + g_{m2}} + R_T\frac{C_1}{C_T}(1-\alpha)] \times \Gamma_{Rt}(\varphi) & \pi - \Phi < \varphi < \pi + \Phi \\ -[\alpha + g_{m2}R_t(1-\alpha)\frac{C_1}{C_T}] \times \Gamma_{Rt}(\varphi) & \pi + \Phi < \varphi < 2\pi - \Phi \end{array} \right\} \tag{46}$$

2. 2. ISF Calculation When C_T Is Big In the case of big C_T, we can replace $\alpha = 0$ in Equation (33) and Equation (46). Thus, the impulse sensitivity functions of cross-connected and tail transistors are simply derived as Equations (47) and (48), respectively.

$$\Gamma_{i_{ds}}(\varphi) = \begin{cases} [1-(g_{m1}-g_{m2})R_t \frac{C_1}{C_T}] \times \Gamma_{Rt}(\varphi) & -\Phi < \varphi < \Phi \\ (1-g_{m1}R_t \frac{C_1}{C_T})\Gamma_{Rt} & \Phi < \varphi < \pi - \Phi \\ [1-(g_{m1}-g_{m2})R_t \frac{C_1}{C_T}] \times \Gamma_{Rt}(\varphi) & \pi - \Phi < \varphi < \pi + \Phi \\ 0 & \pi + \Phi < \varphi < 2\pi - \Phi \end{cases} \tag{47}$$

$$\Gamma_{Tail}(\varphi) = \begin{cases} (g_{m1}-g_{m2})[R_t \frac{C_1}{C_T}] \times \Gamma_{Rt}(\varphi) & -\Phi < \varphi < \Phi \\ [g_{m1}R_t \frac{C_1}{C_T}] \times \Gamma_{Rt}(\varphi) & \Phi < \varphi < \pi - \Phi \\ (g_{m1}-g_{m2})[R_t \frac{C_1}{C_T}] \times \Gamma_{Rt}(\varphi) & \pi - \Phi < \varphi < \pi + \Phi \\ -[g_{m1}R_t \frac{C_1}{C_T}] \times \Gamma_{Rt}(\varphi) & \pi + \Phi < \varphi < 2\pi - \Phi \end{cases} \tag{48}$$

2. 3. ISF Calculation When C_T Is Small Although the impulse sensitivity function of cross-connected and tail transistors has been derived for very small values of C_T in prior works [6, 15], just for the purpose of double checking the derivations obtained in this paper, one can substitute $\alpha = 1$ in Equations (33) and (46) and obtain Equations (49) and (50); those are exactly identical to equations obtained by Andreani et al. [15].

$$\Gamma_{i_{ds}}(\varphi) = \begin{cases} \frac{2g_{m2}}{g_{m1}+g_{m2}} \times \Gamma_{Rt}(\varphi) & -\Phi < \varphi < \Phi \\ 0 & \Phi < \varphi < \pi - \Phi \\ \frac{2g_{m2}}{g_{m1}+g_{m2}} \times \Gamma_{Rt}(\varphi) & \pi - \Phi < \varphi < \pi + \Phi \\ 0 & \pi + \Phi < \varphi < 2\pi - \Phi \end{cases} \tag{49}$$

$$\Gamma_{Tail}(\varphi) = \begin{cases} \frac{g_{m1}-g_{m2}}{g_{m1}+g_{m2}} \times \Gamma_{Rt}(\varphi) & -\Phi < \varphi < \Phi \\ \Gamma_{Rt}(\varphi) & \Phi < \varphi < \pi - \Phi \\ \frac{g_{m1}-g_{m2}}{g_{m1}+g_{m2}} \times \Gamma_{Rt}(\varphi) & \pi - \Phi < \varphi < \pi + \Phi \\ -\Gamma_{Rt}(\varphi) & \pi + \Phi < \varphi < 2\pi - \Phi \end{cases} \tag{50}$$

Comparing ISF obtained for non-small and small C_T from literature [6, 15] reveals that the tail capacitance can reduce phase noise contribution of tail transistor while it adds some terms to Γ_{ids} and may increase phase noise contribution of cross-connected transistors. However, more investigation is presented by numerical values of phase noise for different tail capacitance in Section 3.

3. NUMERICAL AND SIMULATION RESULTS

For more investigation, an LC-tank cross-connected oscillator has been designed and simulated with the circuit parameters shown in Table 1 in a standard 0.18µm CMOS technology. Simulation results show that this oscillator has an oscillation frequency of 5.2 GHz and the power consumption is 8.87 mW. The output voltages are also depicted in Figure 6. In this circuit the switching angle is obtained $\Phi = 50°$.

In continue, the simulated and analytical phase noise of the VCO for different values of tail capacitances are presented and the effect of different values of C_T on phase noise is discussed.

3. 1. Case 1: Non-negligible (Medium) C_T As mentioned before, the noise of cross-connected transistors is cyclostationary and RMS value of each ISF should be calculated by $\Gamma^2_{rms} = \frac{1}{T}\int \Gamma^2(\varphi)d\varphi$. Since, for a given Φ, the integrals have no closed-form expression, their numerical values for different Φ are illustrated. Figs 7(a) and (b) show $\Gamma^2_{i_{ds}-eff-RMS}$ and $\Gamma^2_{Tail-RMS}$ for different values of Φ in the case of C_T=100 fF.

To calculate total phase noise of the circuit by (3), the values of effective ISFs at desired Φ are obtained from Figures 7(a) and (b). The calculated phase noise versus offset frequency for three different tail capacitances and α is shown in Figure 8.

According to Figure 8, in the case of non-negligible tail capacitance, increasing C_T results in phase noise reduction. Also, it indicates that for a given tail capacitance, lower time constant at node *x* (i.e. higher α) is led to better phase noise.

TABLE 1. Circuit parameters for VCO

Parameter	Value
M_{tail}	16 µm/0.18 µm
$M_{1,2}$	26.8 µm/0.18 µm
L_1=L_2	1 nH
R_t	6 Ω
C_1=C_2	0.837 pf
V_{DD}	1.8 V
V_b	1 V

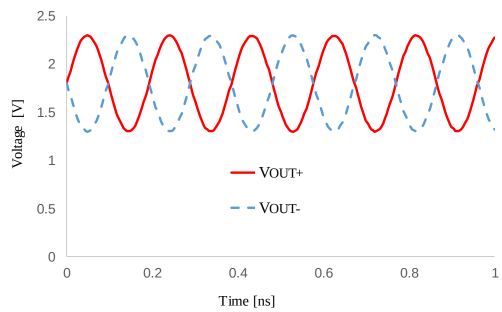
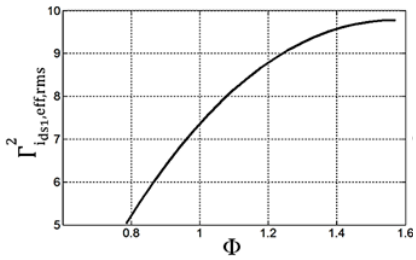
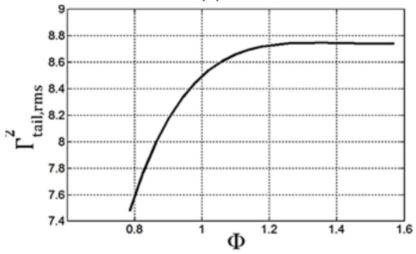


Figure 6. Output waveforms



(a)



(b)

Figure 7. (a) $\Gamma^2_{i_{ds}-eff-RMS}$ and (b) $\Gamma^2_{Tail-RMS}$ vs Φ (radians) for C_T=100 fF

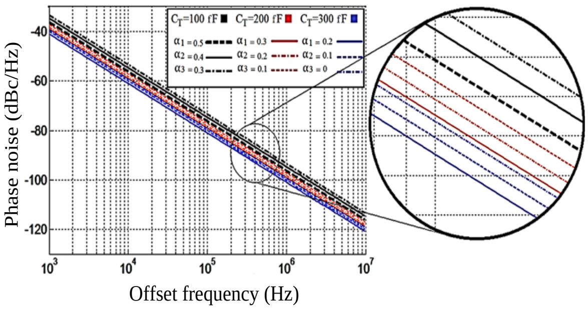
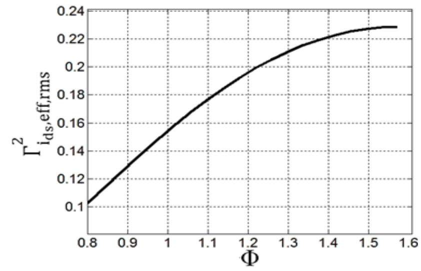


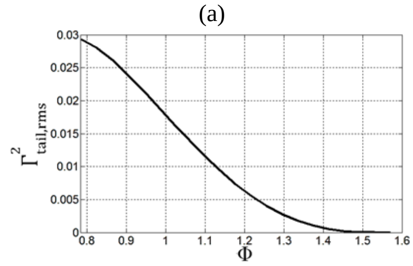
Figure 8. Calculated phase noise for different values of C_T and α when C_T is not negligible.

3. 2. Case 2: C_T Is Big In the case of big tail capacitances, the time constant of the tail node is bigger than the period of oscillation and α=0. Using Equations (39) and (40), numerical values of $\Gamma^2_{i_{ds}-eff-RMS}$ and $\Gamma^2_{Tail-RMS}$ for different values of Φ and C_T=1pF are shown in Figures 9(a) and 9(b), respectively. As expected, the effective ISF of cross-connected transistors (i.e. their noise contribution) in Figure 9 is increased (deteriorated) by increasing Φ. In contradict with Figure 7(b), effective tail ISF for big tail capacitances is decreased by increasing Φ.

Using Equation (3), total phase noise of the VCO for C_T=1pF and $\Phi = 50^\circ$ was calculated using MATLAB software and shown in Figure 10. The simulated phase noise of the oscillator (by ADS) is also depicted in Figure 10 that shows a good agreement with the numerical results.



(a)



(b)

Figure 9. Effective ISF of (a) the cross-connected current and (b) tail transistors vs Φ (radian) for C_T=1pF

According to Figure 11, a bigger tail capacitance is led to a lower phase noise, though for very large C_T increase of C_T has a negligible effect on the phase noise. Therefore, for each VCO, there is an optimum value of C_T in which the tail transistor has lowest contribution to the total phase noise. For example, as shown in Figure 11 the optimum value for C_T is 10 pF and by increasing C_T the phase noise cannot be decreased anymore.

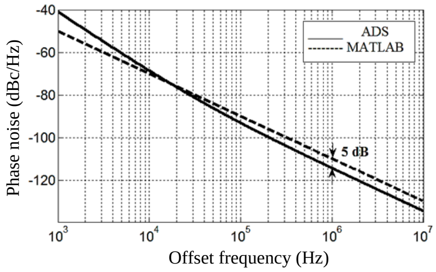


Figure 10. Simulated and calculated Phase noise for C_T=1pF

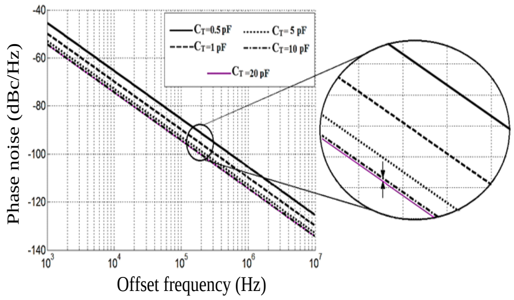


Figure 11. Calculated phase noise for different big tail capacitances

4. CONCLUSION

This paper presented an analytical study of the impact of capacitive filtering on the phase noise in an LC-tank oscillator. Considering the three scenarios for value of C_T the ISF of each transistor has been calculated and the effect of tail capacitance has been discussed. According to the analysis, tail transistor dramatically deteriorates total phase noise and the use of a parallel capacitance can effectively reduce the noise contribution of the tail. It is worth mentioning; the analysis also shows that the time constant of the tail node (x) has a very important role in the amount of noise rejection. While bigger tail capacitance is led to a more noise rejection of tail transistor, it creates a low impedance path and deteriorates the quality factor of LC tank. So, the phase noise caused by cross-connected transistors may be increased. Although the ISF of transistors is usually degraded by increasing conduction angle, our analysis reveals, in the case of large C_T, tail ISF is improved by increasing conduction angle.

5. REFERENCES

1. Chlis, I., Pepe, D., and Zito, D., "Comparative analyses of phase noise in 28 nm CMOS LC oscillator circuit topologies: Hartley, colpitts, and common-source cross-coupled differential pair", ***The Scientific World Journal***, Vol. 2014, (2014), 1–13. doi:10.1155/2014/421321
2. Leeson, D. B., "A Simple Model of Feedback Oscillator Noise Spectrum", ***Proceedings of the IEEE***, Vol. 54, No. 2, (1966), 329–330. doi:10.1109/PROC.1966.4682
3. Hajimiri, A., and Lee, T. H., "A general theory of phase noise in electrical oscillators", ***IEEE Journal of Solid-State Circuits***, Vol. 33, No. 2, (1998), 179–194. doi:10.1109/4.658619
4. Vishwasrao Shinde, S., "Review of Oscillator Phase Noise Models", Proceedings of the International MultiConference of Engineers and Computer Scientists 2014 Vol II, (2014), 1–8.
5. Demir, A., Mehrotra, A., and Roychowdhury, J., "Phase noise in oscillators: a unifying theory and numerical methods for characterization", ***IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications***, Vol. 47, No. 5, (2000), 655–674. doi:10.1109/81.847872
6. Hajimiri, A., and Lee, T. H., "Design issues in CMOS differential LC oscillators", ***IEEE Journal of Solid-State Circuits***, Vol. 34, No. 5, (1999), 717–724. doi:10.1109/4.760384
7. Hegazi, E., Sjöland, H., and Abidi, A. A., "A filtering technique to lower LC oscillator phase noise", ***IEEE Journal of Solid-State Circuits***, Vol. 36, No. 12, (2001), 1921–1930. doi:10.1109/4.972142
8. Samori, C., Lacaita, A. L., Villa, F., and Zappa, F., "Spectrum folding and phase noise in LC tuned oscillators", ***IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing***, Vol. 45, No. 7, (1998), 781–790. doi:10.1109/82.700925
9. Andreani, P., and Sjöland, H., "Tail current noise suppression in RF CMOS VCOs", ***IEEE Journal of Solid-State Circuits***, Vol. 37, No. 3, (2002), 342–348. doi:10.1109/4.987086
10. Jafari, B., and Sheikhaei, S., "Phase noise reduction in a CMOS LC cross coupled oscillator using a novel tail current noise second harmonic filtering technique", ***Microelectronics Journal***, Vol. 65, (2017), 21–30. doi:10.1016/j.mejo.2017.05.003
11. Darabi, H., and Abidi, A. A., "Noise in RF-CMOS mixers: A simple physical model", ***IEEE Journal of Solid-State Circuits***, Vol. 35, No. 1, (2000), 15–25. doi:10.1109/4.818916
12. Grebennikov, A., "Noise Reduction in Transistor Oscillators: Part 2—Low Frequency Loading and Filtering", ***High Frequency Electronics***, (2005), 24–36
13. Ismail, A., and Abidi, A. A., "CMOS differential LC oscillator with suppressed up-converted flicker noise", Digest of Technical Papers - IEEE International Solid-State Circuits Conference, (2003). doi:10.1109/isscc.2003.1234224
14. Samori, C., Zanchi, A., Levantino, S., and Lacaita, A. L., "A fully-integrated low-power low-noise 2.6-GHz bipolar VCO for wireless applications", ***IEEE Microwave and Wireless Components Letters***, Vol. 11, No. 5, (2001), 199–201. doi:10.1109/7260.923027
15. Andreani, P., Wang, X., Vandi, L., and Fard, A., "A study of phase noise in colpitts and LC-tank CMOS oscillators", ***IEEE Journal of Solid-State Circuits***, Vol. 40, No. 5, (2005), 1107–1118. doi:10.1109/JSSC.2005.845991
16. Razavi, B., Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level, (2020), Cambridge University Press.
17. Aghabagheri, R., Miar-Naimi, H., and Javadi, M., "A Phase Noise Reduction Technique in LC Cross-coupled Oscillators with Adjusting Transistors Operating Regions", ***International Journal of Engineering, Transactions A: Basics***, Vol. 33, No. 4, (2020), 560–566. doi:10.5829/IJE.2020.33.04A.07
18. Mazloum, J., and Sheikhaei, S., "1/ f 3 (Close-in) Phase Noise Reduction by Tail Transistor Flicker Noise Suppression Technique", ***Journal of Circuits, Systems and Computers***, Vol. 29, No. 3, (2020). doi:10.1142/S0218126620500358
19. Sun, P., "A low-power and low-phase noise capacitive-degeneration LC VCO", ***International Journal of Electronics Letters***, Vol. 4, No. 4, (2016), 466–471. doi:10.1080/21681724.2015.1082196
20. Andreani, P., and Wang, X., "On the phase-noise and phase-error performances of multiphase LC CMOS VCOs", ***IEEE Journal of Solid-State Circuits***, Vol. 39, No. 11, (2004), 1883–1893. doi:10.1109/JSSC.2004.835828

Persian Abstract

چکیده

این مقاله تأثیر خازن دنباله را روی نویز فاز اسیلاتورهای کنترل‌شده با ولتاژ (LC-VCO) تحلیل می‌کند. در ابتدا روابط عددی نویز فاز به ازای مقادیر مختلف خازن دنباله (C_T) استنتاج شده است و سپس به‌منظور تائید آن، شبیه‌سازی و نتایج عددی باهم مقایسه شده‌اند. برای ساده‌سازی روابط سه حالت کوچک، متوسط و بزرگ برای خازن دنباله در نظر گرفته شده است. در یک مطالعه موردی یک اسیلاتور کنترل‌شده با ولتاژ در فناوری ۱۸۰ نانومتر CMOS طراحی و نتایج عددی برای مقادیر مختلف خازن دنباله ارائه‌شده است. در این مقاله تحلیل‌های عددی نشان می‌دهد که برای C_T =200fF (مقدار متوسط خازن دنباله) و C_T =10pF (مقدار بزرگ خازن دنباله)، مقدار نویز فاز در آفست فرکانسی ۱ مگاهرتز از فرکانس مرکزی ۵/۲ گیگاهرتز به ترتیب برابر dBc/Hz ۹٦- و dBc/Hz ۱۱۸- است. بر طبق نتایج شبیه‌سازی و تحلیل‌های عددی، مقدار تابع حساسیت ضربه (ISF) با افزایش خازن دنباله بهبود می‌یابد. مقادیر عددی همچنین نشان می‌دهد که افزایش بیش‌ازحد خازن دنباله هیچ تأثیری روی نویز فاز ندارد. درحالی‌که انتخاب خازن بزرگ‌تر می‌تواند به‌طور مؤثری نویز فاز کل را با حذف نویز ترانزیستور دنباله کاهش دهد اما تأثیر مسیر امپدانس پایین ایجادشده توسط خازن دنباله نیز می‌تواند نویز فاز را با کاهش ضریب کیفیت تانک خروجی کاهش دهد.