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Control of a Single Stage Boost Inverter Based on Dynamic Sliding Mode Control with Power Decoupling

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ABSTRACT

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Keywords: Boost Inverter Harmonic Rejection Power Decoupling Dynamical Sliding Mode In this paper, the problem of control a single-stage boost inverter is studied. The goal is to achieve a system with robustness against variations in parameters, fast response, high-quality AC voltage, and smooth DC current. To this end, a new type of dynamic sliding mode control is proposed to apply to various scenarios such as parameter uncertainties and DC input voltages. In comparison with the conventional double-loop controllers, the proposed sliding mode controller utilizes only a single loop in its design, while having attractive features such as robustness against parametric uncertainties. In addition, a methodology is proposed for the decoupling of double-frequency power ripples based on proportional-resonant (PR) control to remove the low-frequency current ripples without using additional power components. Compared to conventional controllers, the proposed controller provides several features such as fast and chattering-free response, robustness against uncertainty in the parameters, smooth control, proper steady-state error, decoupled power and good total harmonic distortion (THD) over the output voltage and input currents, and simple implementation. In a fair comparison with classical sliding mode control, simulation results demonstrate more satisfactory performance and effectiveness of the proposed control method.

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1. INTRODUCTION

As a critical component in energy transfer, single-phase Voltage Source Inverters (VSIs) are widely employed in energy storage systems, distributed generation systems, and renewable energy applications such as photovoltaic (PV) systems [1]. Due to inherent variability in renewable energy resources such as solar irradiation, VSIs usually require to provide both boost operation and DC-AC conversion. The main advantage of boost DC-AC inverters is achieving higher output voltage compared to input in a single stage [2]. This converter like other systems has to track a reference signal. Therefore, requires fast response along with robustness under load and variations in input voltage. These conditions increase the control complexity of the boost inverter. Since the boost inverter is composed from two boost DC/DC converters, controlling an AC boost inverter is even more complex. This is motivated an

intense increase in the research in the area of optimal control strategies and resulted in a variety of solutions. To control of the single stage boost inverter, several methods are used such as: Combined fuzzy and adaptive control proposed in literature [3] and A Rule-Based two loop controller analyzed in literature [4] to reduce the second order harmonic of current. Two-loop sliding mode controller was proposed [5] and a classic sliding mode controller, a double-loop control scheme was presented by Özdemir and Erdem [7]. A single loop current control method was used [8] to reduce the harmonic content in the current. A voltage mode control method has been proposed [9].

On the other hand, on the AC side of the single-phase converter, the time-varying instantaneous power flows with the second-order harmonic. If this second-harmonic ripple power is not filtered correctly, it will propagate to

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DC side, which further lowers the efficiency and possibly imposes unintentional stress on the DC source. The undesirable ripples degrade system performance. For instance, they may reduce the maximum power point tracking (MPPT) for the PV panels, leading to light flicker in LED lighting applications that cause overheating of the batteries and decreasing the lifetime of the fuel cell. Second-order power mismatch between DC and AC sides must be handled through a mechanism generally known as "power decoupling" [10]. In this regard, the filtering methods are divided into two main categories: passive methods and active methods. Both methods are based on additional components, which in turn, increase the system complexity and cost while adding losses to the system that reduce the overall inverter efficiency [10-12]. Due to nonlinearities in the converter, harmonic generation is unavoidable. These harmonics are the major output quality issues. In other words, it is crucial to control the harmonics generated by these inverters to limit their adverse effects on the quality of the output voltage [10]. Therefore, to avoid creating harmonics, the controller must provide a high-quality sinusoidal output with minimal distortions [13, 14].

In this paper, instead of the traditional approach of controlling boost inverter, a novel control method is proposed to achieve the mentioned objectives. In this regard, a new dynamical sliding mode with delay compensation is initially presented to track the appropriate reference. Then, an innovative solution with no additional power electronics components is proposed to ensure the decoupling of the double frequency pulsating power. Finally, selected voltage harmonics are compensated using additional PR controllers to perform at particular harmonic frequencies to either reduce or eliminate them. The paper is organized as follows. Section II describes the boost inverter model. The proposed decoupling and harmonic rejection solutions and control are discussed in Section III, while simulation validation is presented in Section IV. Finally, Section V highlights the main paper contributions and concludes the study.

2. MODEL DESCRIPTION

The boost DC–AC inverter, also known as the boost inverter, is specifically interesting due to its capability in generating AC output voltages higher than the input DC voltage in just a single stage. The circuit implementation of the proposed boost inverter is illustrated in Figure 1 [15].

In Figure 1, S_1 , S_2 , S_3 , and S_4 are power switches, L_1 , L_2 , C_1 , C_2 , and R_{out} are individual inductors and capacitors in boost converters, and the equivalent load in the output terminal, respectively. Moreover, v_1 , v_2 , v_{in} , and V_{out} are individual output voltages



Figure 1. Circuit framework of single-stage boost inverter

for the two boost converters, and the input and output voltages for the boost inverter, respectively. As shown in Figure 1, the proposed inverter is composed of two conventional DC-DC converters, along with a connected load. In this topology, converters are driven by two 180° phase-shifted DC-biased sinusoidal references, while each generates a DC-biased Sine wave on the output, namely v_1 and v_2 , respectively. In other words, each source generates a unipolar voltage to maximize the voltage excursion across the load.

The converter output voltages (v_1 and v_2), and the inverter output voltage (V_{out}) can be represented by

$$v_{1} = V_{dc} + V_{m} \sin\theta$$

$$v_{2} = V_{dc} + V_{m} \sin(\theta + \pi)$$

$$V_{out} = v_{1} - v_{2} = (V_{m} + V_{m}) \sin\theta = 2V_{m} \sin\theta$$
(1)

where V_{dc} is the DC offset voltage of each boost converter. To model the system dynamics, it is assumed that all the circuit components are ideal and that the boost inverter operates in a continuous conduction mode (CCM). The duty cycle D is defined as the time scale when switch S_2 is ON, while the duty cycle D' is the time scale when the switch S_4 is ON. According to this definition, the switch S_1 is ON during the time-scale 1 – D and the switch S_3 in 1 - D'. When S_2 and S_4 are ON and S_1 and S_3 are OFF, the input power source v_{in} charges the inductors L_1 and L_2 , and the capacitors C_1 and C_2 discharge to the output terminals v_1 and v_2 , respectively. On the contrary, when S_1 and S_3 are ON and S_2 and S_4 are OFF, inductors L_1 and L_2 discharge to the capacitors and the output terminals. Consequently, by employing the averaging concept and the Kirchhoff's laws, the nonlinear state-space model for the boost inverter circuit with the stated variables can be obtained [15].

$$L_{1}\frac{di_{1}}{dt} = V_{in} - Dv_{1} C_{1}\frac{dv_{1}}{dt} = Di_{1} - \frac{v_{1} - v_{2}}{R_{out}} L_{2}\frac{di_{2}}{dt} = V_{in} - D'v_{2} C_{2}\frac{dv_{2}}{dt} = D'i_{2} + \frac{v_{1} - v_{2}}{R_{out}} V_{out} = v_{1} - v_{2}$$
(2)

where i_1 and i_2 are the currents for the inductors L_1 and L_2 , while v_1 and v_2 are capacitor voltages. As stated earlier, v_{in}, V_{out}, D , and D' are the input DC voltage, output AC voltage, and the switching duty cycles,

respectively. The objective is to design switching pattern for D and D', such that:

$$V_{out} \rightarrow v_{ref} = Vsin(\omega t)$$

$$i_1 + i_2 \rightarrow I_{DC}$$
(3)

with proper convergence speed and robustness under load, along with input-voltage variation and no power coupling and harmonics problems. Parameters V and ω are the amplitude and the frequency of the desired AC voltage, respectively.

3. PROPOSED CONTROL

In this study, two types of compensators are implemented, namely dynamic sliding-mode control for the voltage tracking and PR compensators for power decoupling and harmonic rejection. In the proposed strategy, control inputs (D and D') are generated according to the converter currents and voltages. The closed-loop system (based on the proposed controller) is comprised of two parts: the differential inverter and the control blocks. The control blocks contain a sliding-mode controller and two PR compensators. The control system is employed to track the following control objectives for the differential converter: 1) output voltage control, 2) power decoupling and 3) harmonic rejection.

3.1. Reference Tracking The initial objective for the control problem is to design suitable control inputs (D and D') to enforce the system output to track a sinusoidal reference v_{oref} , with the possible occurrence of uncertainties in the system. In other words, the proposed controller for the single-stage boost inverter aims to force the system states v_1 and v_2 to track reference output voltage for their respective converter $(v_{1ref} \text{ and } v_{2ref})$. The two reference voltages are determined from the v_{oref} , DC input voltage, and nominal value of the states. Therefore, to control the single-stage boost inverter more effectively, a new dynamic sliding-mode control is proposed to minimize the error and adjust the duty cycle for the switches to ensure the system's stability. Moreover, it provides attractive features such as fast dynamic response, insensitivity to variations in plant parameters and external disturbance, and elimination of the chattering problem in practical senses. The performance of the proposed system is compared with the conventional sliding mode controller under different operating conditions. Therefore, in the following subsections, first, the Classical Sliding Mode Control (CSMC) and then the proposed Dynamic Sliding Mode Control (DSMC) is introduced.

Consider a continuous-time nonlinear model for the boost inverter described by the state-space representation as Equation (2). By defining $x = [x_1 \ x_2 \ x_3 \ x_4]^T =$

 $[i_1 \ v_1 \ i_2 \ v_2]^T$ is the state vector while $y = [v_1, v_2]$ and $u = [u_1; u_2] = [D; D']^T$ are the output and input vectors, respectively. In CSMC, the control objective is to drive the output voltages to the desired values. In CSMC, the sliding surface can be chosen as [8]:

$$s_{i} = \sum_{k=0}^{r_{i}-1} \lambda_{k}^{(i)} (y_{i} - y_{i}^{d})^{k}, for \ i = 1, \dots, r_{i} - 1$$
(4)

where y_i^d is the desired output, r_i is the relative error e_i , and $e_i^{(k)}$ is the k^{th} order derivative of the error. The control objective can be achieved by pushing the sliding surfaces (4) to zero.

In this paper, to control of boost inverter, a dynamic sliding mode control (DSMC) is proposed to perform the current-mode control. In this scheme, the controller focuses on the generating of AC voltage on the load rather than on the capacitors. The sliding surfaces are defined by:

$$s_{1} = i_{1} + k_{p1}(v_{1} - v_{ref1}) + k_{i1} \int_{0}^{t} (v_{1} - v_{ref1}) d\tau$$

$$s_{2} = i_{2} + k_{p2}(v_{2} - v_{ref2}) + k_{i2} \int_{0}^{t} (v_{2} - v_{ref2}) d\tau$$
(5)

Theorem 1: The control law (6) pushes the sliding surfaces (5) to zero:

$$D = h_1^{-1} (x) (D_{eq} + K_1 sign(s_1))$$

$$D' = h_2^{-1} (x) (D'_{eq} + K_2 sign(s_2))$$
(6)

where

$$D_{eq1} = \frac{v_{in}}{L_1} + k_{p1} \left(-\frac{x_2 - x_4}{RC_1} - \dot{x}_{2ref} \right) + k_{i1} \left(x_2 - x_{2ref} \right) D'_{eq1} = \frac{v_{in}}{L_2} + k_{p2} \left(\frac{x_2 - x_4}{RC_2} - \dot{x}_{4ref} \right) + k_{i2} \left(x_4 - (7) + x_{4ref} \right) h_1 \left(x \right) = \left(\frac{x_2}{L_1} - \frac{x_1 k_{p1}}{C_1} \right) h_2 \left(x \right) = \left(\frac{x_4}{L_2} - \frac{x_3 k_{p2}}{C_2} \right)$$

and k_{pi}, k_{ii} and $K_i, i = 1, 2$ are positive constants and $\frac{x_2}{L_1} \neq \frac{x_1k_{p1}}{C_1}, \frac{x_4}{L_2} \neq \frac{x_3k_{p2}}{C_2}.$

Consider the following Lyapunov function:

$$V = \frac{1}{2}ss^{T} = \frac{1}{2}(s_{1}^{2} + s_{2}^{2})$$
(8)

the derivative of V is:

$$\dot{V} = s_1 \dot{s_1} + s_2 \dot{s_2}$$
 (9)

by substituting Equation (7) into Equation (6), we have

$$\dot{s} = \begin{pmatrix} K_1 sign(s_1) \\ K_2 sign(s_2) \end{pmatrix}$$

$$\dot{V} = -s^{\mathrm{T}} \begin{pmatrix} K_1 sign(s_1) \\ K_2 sign(s_2) \end{pmatrix} = -K_1 s_1 s \operatorname{ign}(s_1) - K_2 s_2 \operatorname{sign}(s_2) = -K_1 |s_1| - K_2 |s_2| < 0$$
(10)

Since K_1 and K_2 are positive, $\dot{V} < 0$. As a result, the Lyapunov function *V* approaches zero and thus, s_1 and s_2 (as the sliding surfaces) approach zero as well. **Remark**

If $h_1(x)$ and $h_2(x)$ are zero, D and D' are given by

Equation (11)

$$D = \frac{k_{p1} V_{in} + \frac{v_1 - v_2}{R}}{i_1 + k_{p1} v_1}$$

$$D' = \frac{k_{p2} V_{in} - \frac{v_1 - v_2}{R}}{i_2 + k_{p2} v_2}$$
(11)

3.2. Power Decoupling In recent years, many of the proposed methods have aimed to eliminate lowfrequency current ripples. According to literature [7,8] large electrolytic capacitors are utilized to suppress the current ripples. However, the electrolytic capacitor is likely to increase both the system's size and cost. Moreover, since electrolytic capacitors are devices with limited operating lifetime, they will also shorten the lifetime of the system. Various power decoupling techniques are discussed that require additional power components and energy storage elements to perform as power decoupling circuits and thus, are not preferred [12]. To overcome such shortcomings, a Proportional Resonant (PR) control method is proposed in this paper to eliminate the low-frequency current ripple of the boost inverter systems without using additional power components or electrolytic capacitor. The PR controller provides an infinity gain at a particular frequency (resonant frequency), while almost unity gain in other frequencies. A PR controller comprises of two parts, namely proportional and resonant, as expressed in Equation (12).

$$G_{PR}(s) = K_P + \frac{K_I}{s^2 + \omega_0^2}$$
(12)

where ω_0 is the resonant frequency, K_P is the proportional gain and K_I is the integral gain. Since there exists high gain at a narrow band surrounding resonant frequency, the PR controller is capable of eliminating steady-state error. Note that K_I is related to bandwidth, and K_P determines the phase of bandwidth and gain margin. Since the objective in power decoupling is eliminating the second-order ripple current, a second-order PR controller G_{PR2} is employed to realize the zero-error tracking, defined as:

$$G_{PR2}(s) = K_{P1} + \frac{K_{I1}}{s^2 + (2\omega_0)^2}$$
(13)

3.3. Harmonic Rejection The distributed power generation systems generate harmonics due to the non-linearities in their converters. Moreover, such systems have major output quality issues, mainly due to the fact that the number of systems connected to the inverter is always increasing, indicating the significance of controlling the harmonics generated by these inverters to limit their adverse effects on the output voltage quality [13-14]. Therefore, to reject harmonics, the controller must be capable of providing high-quality sinusoidal

output with minimal distortion. Selected harmonics in the voltage, including the 3rd, 5th, 7th, etc., can be compensated by additional PR controllers at particular harmonic frequencies. This compensation reduces the THD; therefore, the inverter is compliant with the IEEE and IEC standards [16]. In this paper, a selective harmonic compensator is designed to eliminate the 3rd harmonic. Then, a 3rd-order PR controller is employed defined by the transfer function as:

$$G_{PR3}(s) = K_{P2} + \frac{K_{I2}}{s^2 + (3\omega_0)^2}$$
(14)

The closed loop system block diagram is illustrated in Figure 2.

As shown in Figure 2, the proposed control scheme is divided into three stages: the first stage consists of dynamic sliding control method in which transient behavior improvement and closed loop stability. Then the PR control concept is employed to eliminating the second-order ripple current in second stage and to reject harmonics in last stage.

4. SIMULATION RESULTS

The proposed controller is investigated through numerical simulation based on the nominal values provided in Table 1. Simulation results provided in this section are performed using Matlab/Simulink software. Delays are generally created by different factors. In boost inverters, calculation time and the PWM section are responsible for a delay time as large as approximately 1.5 times the sampling time. Therefore, simulations in this section are performed with consideration of delays, which makes it more difficult to obtain satisfactory performance and stability. For the sake of a fair comparison, the performance of the classical sliding mode control is simulated with similar values.

To verify the effectiveness of the proposed controller in decreasing the steady-state error, the reference and the rated performances of the boost-inverter is demonstrated



Figure 2. The Block Diagram of Proposed Closed-loop system

in Figure 3. The boost inverter is modeled in Equation (2), and is controlled by the dynamical SMC (DSMC) proposed in Euations (6) and (7).

To examine the performance of the controller against uncertainty, the system is initially simulated under load variations.

To this end, the load utilized in the simulation is changed according to a step function at the 0.06th second. The results are illustrated in Figure 4. It can be seen that the controller is robust under large load variations, since the output voltage remains stationary and the system recovered very fast.

In order to evaluate the robustness of the proposed strategy, concerning parameter uncertainties, simulation is performed under variation of c_1 from 100µF to 70µF at the 0.1th second as shown in Figure 9. In this case, the circuit is asymmetric. It is observed in Figure 5 that the considered variations do not impose significant effects on the output voltage for both DCSM and CSMC; however the error for CSMC is significantly more than DSMC technique.

To evaluate the performance of the controller under variation of the input voltage, where it drops from 48 to 38 at the 0.1th second. The simulation results are presented in Figure 6. Note that the DC component of the voltage on the capacitors is automatically adjusted when the input voltage changes. It should be pointed out that this perturbation rejection is achieved without input voltage measurement.

Figure 6 shows that however the error of DSMC does not change visibly, but the error of CSMC goes up sharply and does not come down.

TABLE 1. System parameters	
Symbol	Value
L_{1}, L_{2}	1mH
<i>C</i> ₁ , <i>C</i> ₂	$100 \mu F$
V _{in}	48volt
Voref	$120\sqrt{2}\sin(120\pi t)$
R	100Ω



(right) of the proposed DSMC and CSMC



Figure 4. Performance of the proposed DSMC and CSMC under 50% load variation at second 0.06th Output Voltage (top-left), Steady state error (top-right), Output Current (bottom)







Figure 6. Performance (left), Steady state error (right) of the proposed DSMC and CSMC under 20% input voltage variation at 0.1th second

In the second part of the simulations, the power decoupling was evaluated for the boost inverter, according to the parameters listed in Table 1. In Figure 7,



Figure 7. Simulation Result and FFT analysis of the input current ide applying DSMC without power decoupling

the result without power decoupling is demonstrated, while Figure 8 illustrates the condition in which power decoupling is considered.

As anticipated, without decoupling, the capacitors c_1 and c_2 in Figure 7 contain only a DC offset and an AC component at the fundamental frequency. Therefore, the DC offset cancels each other differentially, while the AC component is doubled at ω . Thus, the AC voltage is appropriate, while the DC input current i_{dc} is not constant. Consequently, power decoupling is necessary and as expected, using the proposed power decoupling technique, the second order component in the DC side is dramatically reduced to almost zero.

As can be seen in Figures 8 and 9, when the power decoupling is enabled, i_{dc} becomes constant and creates 3^{rd} order harmonics on the output AC voltage. Therefore, the harmonic rejection is necessary at 3ω to produce the desired AC voltage and current waveforms. As expected, in Figure 10, using aforementioned harmonic compensator is lead to desired ac voltage withot 3^{th} order harmonic. However The 3^{rd} order harmonic compensator creates 4^{th} order harmonic on i_{dc} . Therefore, the power decoupling technique must be capable of reducing this harmonic. The extended power decoupling is hence necessary and as expected, employing the proposed power.

Figure 11 shows that 4th order harmonic on i_{dc} is disappeared when the extended power decoupling is enabled. To get an overview of the performance of the closed loop system, the value of THD in the output voltage in different simulation scenarios are presented in Table 2.

As can be seen in last scenario of Table 2, when the 4th order power decoupling is enabled, the value of THD in the output voltage has increased because 4th order power decoupling creates 5th order harmonics on the output AC voltage.



Figure 8. Simulation result and FFT analysis of the input current i_{dc} applying proposed DSMC with power decoupling



Figure 9. Simulation result and FFT analysis of the output voltage v_{ac} applying proposed DSMC and power decoupling



Figure 10. Simulation result and FFT analysis of the output voltage v_{ac} applying proposed DSMC, power decoupling, and 3^{rd} order harmonic compensator



Figure 11. Simulation result and FFT analysis of the input current i_{dc} applying proposed DSMC, extended power decoupling and 3^{rd} order harmonic compensator

TABLE 2. THD of output voltage in different simulation scenarios

Seconorios	THD%	
Scenarios	i _{dc}	Vout
Without Power Decoupling and Harmonic Rejection	178.72	1.2
With Power Decoupling and Without Harmonic Rejection	25.87	2.94
With Power Decoupling and Harmonic Rejection	46.82	.95
With Extended Power Decoupling and Harmonic Rejection	25.14	1.51

5. CONCLUSION

This paper aimed to develop a dynamic sliding-mode control scheme for a single-stage boost inverter with power decoupling and harmonic rejection capabilities. This controller consists a dynamic sliding-mode controller proposed with a single loop to overcome uncertainties, time-delay and two Proportional Resonant (PR) current controllers with additional selective harmonic compensators which employed to achieve selected harmonic rejection of the output voltage and compensate the 2nd and 4th order ripples. Simulations on the inverter confirmed the effectiveness of the DSMC in providing several features such as fast and chattering-free response, robustness against uncertainty in the parameters, smooth control, proper steady-state error, decoupled power and good total harmonic distortion (THD) around 1.5% over the output voltage, and simple implementation. Plus, the effectiveness of the PR controllers in reducing selected harmonics in the input current and output voltage are demonstrated. Using this power decoupling scheme, smooth DC current and highquality AC voltage can be obtained Moreover, to provide a fair comparison, the performance of the classical sliding mode control was simulated. As can be seen, using CSMC leads to high steady state error, which confirms that the error in CSMC was higher than DSMC.

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Persian Abstract

چکيده

در این مقاله مسئله کنترل اینورتر افزاینده تک مرحله ای مورد بررسی می گیرد. هدف از کنترل در این مقاله، داشتن یک سیستم با پاسخ سریع، ولتاژ AC خروجی با کیفیت بالا، جریان DC صاف و مقاوم در برابر تغییر پارامترها است. برای این منظور نوع جدیدی از کنترل مود لغزشی دینامیکی ارائه می شود تا بر عدم قطعیت های پارامتری و تغییرات ولتاژ ورودی DC به خوبی غلبه کند. در مقایسه با کنترل کننده های دو حلقه ای مرسوم، کنترل کننده مود لغزشی پیشنهادی در این مقاله در حالیکه ویژگیهایی از قبیل مقاوم بودن در برابر عدم قطعیتهای پارامتری را ارائه می دهد، تنها از یک حلقه در طراحی خود استفاده می کند. به علاوه در این مقاله از یک روش مبتنی بر کنترل تناسبی-مواوم بودن در برابر عدم قطعیتهای پارامتری را ارائه می دهد، تنها از یک حلقه در طراحی خود استفاده می کند. به علاوه در این مقاله از یک روش مبتنی بر کنترل تناسبی-رزونانسی نیز برای دکوپله سازی توان در فرکانس های مرتبه زوج استفاده می شود تا ریپل جریان فرکانس پایین را بدون استفاده از المانهای قدرت یا خازنهای الکترولیت اضافی محدود کند. در مقایسه با کنترل کننده های مرتبه زوج استفاده می شود تا ریپل جریان فرکانس پایین را بدون استفاده از المانهای قدرت یا خازنهای الکترولیت اضافی محدود کند. در مقایسه با کنترل کننده های مرسوم، کنترل کننده پیشنهادی در این مقاله ویژگیهای مطوبی از جمله پاسخ بدون وزوز ، کنترل نرم، خطای حالت ماندکار مناسب، توان دکوپله و اعوجاج هارمونیکی کل مناسب در جریان ورودی و ولتاژ خروجی را در کنار پیاده سازی ساده ارائه می دهد. در یک مقایسه عادلانه با کنترل مود لغزشی کلاسیک، نتایج شبیه سازی، عملکرد و اثربخشی روش پیشنهادی را نشان میدهند.