



A Phase Noise Reduction Technique in LC Cross-coupled Oscillators with Adjusting Transistors Operating Regions

R. Aghabagheri, H. Miar-Naimi*, M. Javadi

Department of Electrical and Computer Engineering, Babol Noshirvani University of Technology, Babol, Iran

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ABSTRACT

In this paper, an intuitive analysis of a phase noise reduction technique is done, and then a modified structure is proposed to achieve higher phase noise reduction than the original one. This method reduces the impact of noise sources on the phase noise by decreasing closed-loop gain in zero-crossings points and moving this high closed-loop gain to the non-zero-crossings points. This reduction tested on different scales and all of them showed improvement in the phase noise performance. In other words, this method reduces the phase noise by manipulating the operation region. Impulse sensitivity function (ISF) for the proposed structure shows degradation in comparison to the original structure. We have designed the proposed oscillator in 0.18 μm using CMOS TSMC standard technology. The proposed oscillator operates on 900 MHz, moreover, phase noise is -138.4 dBc/Hz at 1 MHz offset frequency while it consumes 3.11 mA from 1.8 V supply voltage.

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1. INTRODUCTION

In recent years, wireless technologies and telecommunications have been used in the daily lives of humankind. Oscillators are one of the main blocks in RF communication, and their performance affects the entire systems. Phase noise is one of the most important parameters for evaluating oscillators. A high amount of phase noise can destroy a part of the transmitted information and cause interference with surrounding bands. Designing a low phase noise oscillator is usually a challenging task.

To reduce the phase noise of the oscillators, various methods are introduced till now. One way to overcome the phase noise problem, named current shaping method, decreases the current of the oscillator when the output voltage is in the zero-crossings points. The advantages of this method compared to other existing techniques are their relatively less occupied area and also their lower power consumption [1]. Although this method decreases phase noise, the achieved results in this method are

usually less optimal than the noise filtering method with a combination of inductors and capacitors [1-5].

However, implementing methods using inductors requires much space; a new structure is proposed that utilizes a kind of filtering that just needs extra capacitors. The structure introduced in literature [6] illustrated in Figure 1. In this figure, a phase shift is created by the C_{cpl} between the drain and the gate voltage waveform of the NMOS transistors. In addition, a pair of PMOS is implemented to make the output more rectangular.

Although this method has an acceptable impact on phase noise, as will be presented in this paper, the PMOS pair plays a major role in ISF at zero-crossings points.

In this work, we investigated the effect of transistors regions on the ISF in various phases of oscillation. The simulations indicate a low loop gain at zero-crossings points can significantly decrease the ISF at these points. Based on the mentioned investigation, we have significantly improved the ISF and the phase noise by minor changes in the proposed oscillator [6]. The phase noise reduction technique is introduced by Oh [6] in

*Corresponding Author Email: h_miare@nit.ac.ir (H. Miar-Naimi)

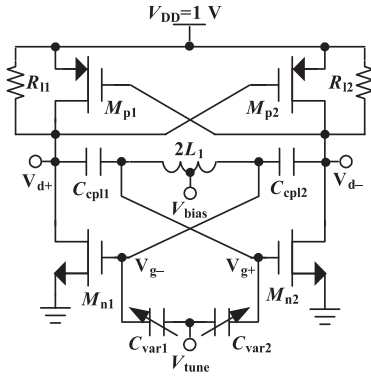


Figure 1. Low phase noise Oscillator with a series LC resonator

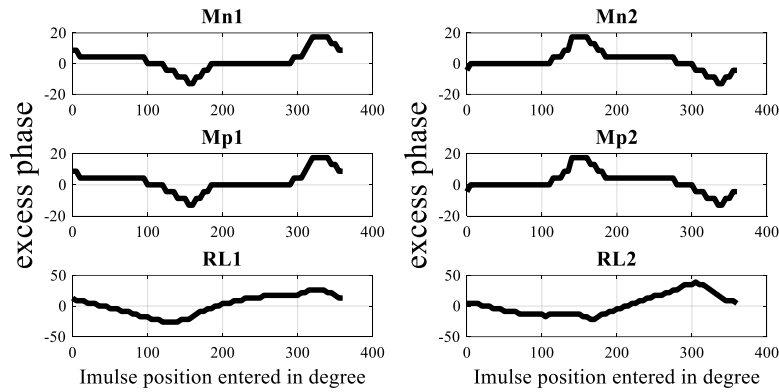


Figure 2. ISF for the oscillator of Figure 1

waveforms. This phase shift decreases the ISF. Besides, the PMOS pair adds more negative resistance to the structure and makes the output waveform more rectangular. It should be noticed that a square-wave waveform has usually a lower ISF than a sine-wave waveform [6].

Knowing the noise sources and their contribution to the generated phase noise is necessary for analyzing the phase noise. In this paper linear and time-varying model introduced by Haji-Miri et al. [7] is used to get some insight into the phase noise of this structure. In this model, the impulse response of the circuit is obtained by assuming that the conversion of noise to the phase noise is a linear function. Equation (1) is used for calculating The gamma function using impulse response.

$$h_{\phi}(t, \tau) = \Gamma(\omega_0 \tau) \frac{u(t - \tau)}{q_{max}} \quad (1)$$

Where $u(t - \tau)$ is the unit step at $t = \tau$, and q_{max} denotes the maximum injected charge due to the current impulse. Also, moreover, Γ represents the ISF which is a dimensionless and periodic function with a period of 2π . Finally, $\Gamma(\omega_0 \tau)$ shows how much phase shift occurs from applying a unit impulse at time $t = \tau$.

section 2. In section 3, we discuss how the proposed oscillator reduces the phase noise and then we calculated the phase noise and the oscillation frequency in this section. The simulation results are also shown in section 4. Finally, section 5 is devoted to the conclusion.

2. STRUCTURE ANALYSIS OF OSCILLATOR

In Figure 1, The C_{var} and the L_1 , which are parallel, determine the frequency of the oscillator. C_{cpl} in series with L_1 generates a filter to suppress the noise. Moreover, C_{cpl} causes a phase shift between the drain and the gate

Figure 2 demonstrates the ISF of the oscillator in a period of 2π . It should be noticed that the vertical axis shows the excess phase remains in the output waveform. In the conventional LC oscillator, the ISF peak is at 0 and 180 degrees. However, in this circuit, as mentioned before, C_{cpl} causes a phase shift between the gate and the drain waveform. Therefore, gamma peaks are slightly distanced from these points.

According to the linear and time-varying model introduced by Haji-Miri et al. [7] at the zero-crossings points, all the noise is transmitted to the output phase. To get more details, the operation regions of each four transistors over a full period of 2π from 0 to 360 degrees is examined. In conventional oscillator design, at the zero-crossings points, all the transistors are in saturation region generally; however, as shown in Figure 3 the NMOS transistors are not in the saturation region simultaneously because of the phase shift technique[6], thus the loop gain and the phase noise in the zero-crossings is less than a conventional design.

As shown in Figure 3, at the zero-crossings, the PMOS pairs and one of the NMOSs are in the saturation region. Although the loop gain is reduced because of an NMOS which is in the cut-off region at this moment, the



Figure 3. Transistors operation region in a period for the oscillator of Figure 1

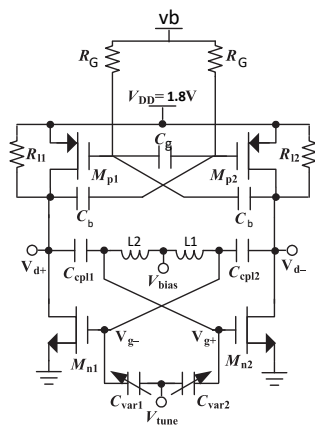


Figure 4. Proposed LC oscillator

loop gain is still high since the impedance seen by the drain of the transistors is high. It means noise can be amplified frequently in this positive loop and transferred directly to the phase. Therefore, not only the PMOS pair make the output waveform more rectangular but also generates positive feedback with high loop gain which is not desirable. Moving the high closed-loop gain to low sensitive phases helps to reduce the RMS value of the ISF.

3. PROPOSED OSCILLATOR DESIGN

The proposed oscillator structure is depicted in Figure 4. Where C_b is DC blocker and C_g is AC divider. To explain how this method works the operation region of all the transistors is plotted in Figure 5. At zero-crossings points, the PMOS pair are in the saturation region. However, the NMOS transistors are alternately in the triode region. In comparison with the original oscillator, the operation region of the NMOS pair is changed from saturation to the triode in the transition region. This alteration reduces output resistance of the NMOS that results in decreasing the loop gain which reduces the amplification of noise at zero-crossings points and improves the phase noise. It is noticeable that high loop gain is needed to generate oscillation. As shown in Figure 5, there are regions in which three of the transistors are operating in the saturation region, but these regions are away from zero-crossings points, where noise has the maximum effect on phase. The high loop gain which was occurred at zero-crossings points was transferred to the non-zero-crossing points. The Trans-conductance of the NMOS pair is much bigger than of PMOS pair. Thus, when both pairs are in saturation, the gain of the NMOS pair is bigger than the PMOS pair. For example, in Figure 5 around 130 to

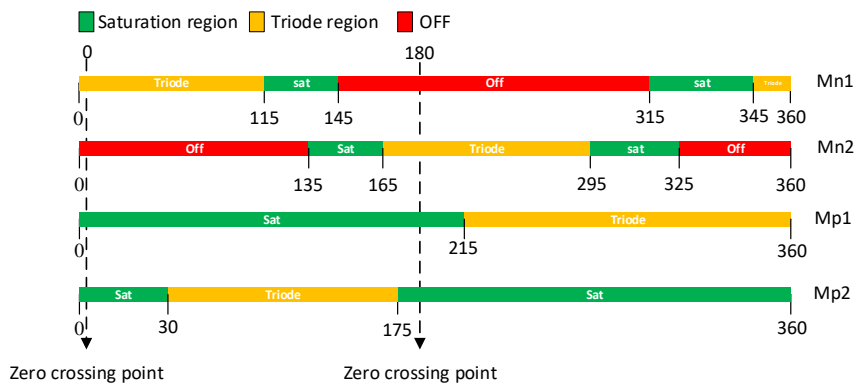


Figure 5. Transistors' operating region in a period for the proposed Osc

150 degrees both NMOS transistors and one of the PMOS transistors are in the saturation region, which according to the high loop gain in this region, the ISF has the maximum value at this point (Figure 6). Whereas this point is not zero-crossings points, its impact on the phase is low. Hence, the ISF of the proposed circuit is significantly less than the ISF of the original one.

For example, due to Figure 7 with some insight into the structure introduced in [6], the distributed noise on vd_+ propagates on the gate of Mn_2 and Mp_2 . These two transistors are in the saturation region at the zero-crossings points according to Figure 3. In this sensitive moment (zero-crossings points), noise amplifies with a saturation region gain. Considering the proposed structure, we designed in Figure 7, from the first route, noise attenuates with divider capacitors and then it reaches the gate. Noise in the second route, which is shown with green color, reaches to the gate of Mn_2 . In the proposed structure, Mn_2 is in the triode region which means it is not in the amplification mode at the zero-crossings points. Since Mn_2 is in triode, the output resistance on vd_- is significantly dropped by Mn_2 in comparison with the introduced structure in [6]. Because of low output impedance on vd_- , Mp_2 , which is in the saturation region, has less amplification than the original structure. C_b and C_g reduce the effective trans-

conductance of the PMOS pair by α factor where α is the voltage division factor between C_b and $2C_g$ and equals to ($\alpha = \frac{C_b}{C_b + 2C_g}$). It is noticeable that this reduction leads to a lower loop gain. Although loop gain reduction can help to ISF reduction at the zero-crossings points, it decreases the slope of the output waveform at this point. Moreover, loop gain reduction decreases the output amplitude which results in higher phase noise. Therefore, there is an optimum point for α . The phase noise for different values of α in terms of different values of V_b is simulated and the results are presented in Figure 8, which shows that for each bias voltage, in certain α , it gives the best phase noise performance.

3. 1. Calculating Phase Noise

With the RMS

value of the Γ function phase noise can be calculated according to Equation (2) [7].

$$L(\Delta\omega) = 10 \log \frac{\Gamma_{RMS}^2 i_n^2 / \Delta f}{q_{max}^2 4\Delta\omega^2} \tag{2}$$

$$q_{max} = CV_{max} \tag{3}$$

where, $i_n^2 / \Delta f$ is the white power spectral density q_{max} denotes the maximum charge displacement across the capacitor on the output node and $\Delta\omega$ is the offset

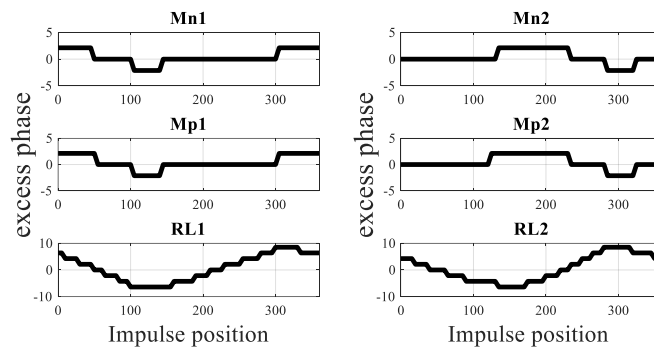


Figure 6. ISF of the proposed Osc

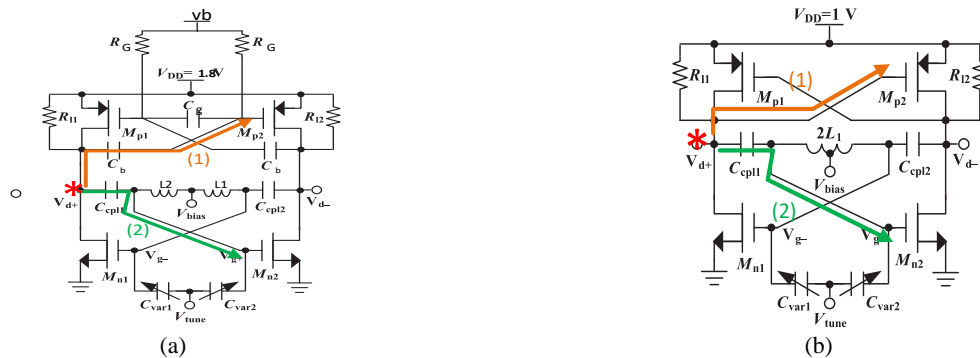


Figure 7. noise contribution from V_{d+} to PMOS and NMOS gate of a) the proposed structure b) the introduced structure in [6]

frequency from the oscillation frequency. Table 1 Presents the Γ_{RMS} of both oscillators in degrees and the calculated phase noise performance using Equation (2) for verifying the accuracy of the Γ_{RMS} is depicted in Figure 9 which is consistent with the simulation result for both mentioned oscillators. The figure indicates a 6 dB improvement in 1 MHz offset frequency in the same condition.

3. 2. Oscillation Frequency Node analysis helps to calculate the oscillation frequency of the proposed oscillator. To simplify the calculations, the half-circuit model is prepared which is presented in Figure 10 KCL equations at $V_1, V_2,$ and V_3 nodes give us the admittance matrix which obtained in Equation (4).

$$\begin{pmatrix} sC_{var} + \frac{1}{LS} - sC_{cpl1} & -sC_{cpl1} & 0 \\ -g_{mn} + sC_{cpl1} & sC_b + sC_{cpl1} & -g_{mp} - sC_b \\ 0 & sC_b & 2sC_g + sC_b \end{pmatrix} \times \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} \quad (4)$$

The oscillation frequency obtained in Equation (5) by putting the imaginary part of the determinant equal to zero.

$$f = \frac{1}{2\pi} \frac{\sqrt{C_{cpl1}^2 - 2C_g C_{cpl1} + 2C_b C_g}}{\sqrt{L(C_{var} - C_b)(C_{cpl1}^2 + 2C_g C_{cpl1} + \frac{2C_b C_g C_{var}}{C_{var} - C_b})}} \quad (5)$$

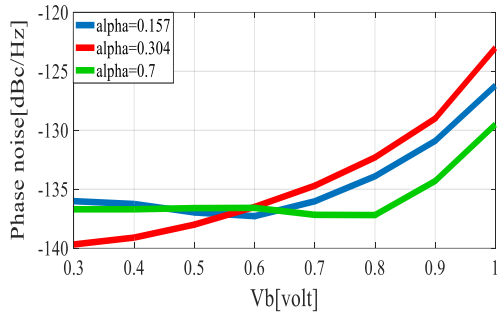


Figure 8. Phase noise variation in terms of bias voltage with different α

TABLE 1. Γ_{RMS} for the mentioned Osc. in degree

	$\Gamma_{RMS_{Osc.of Fig.1}}$	$\Gamma_{RMS_{proposed}}$
Mn1	7.0422	2.7278
Mn2	6.8360	2.6353
Mp1	7.0422	2.7729
Mp2	6.8360	2.7278
R1	16.1459	10.1722
R2	16.9384	9.8749

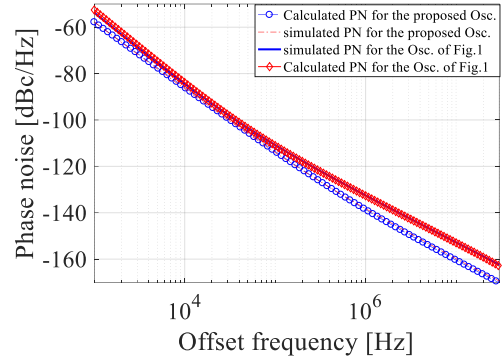


Figure 9. The simulated and calculated phase noise of the mentioned oscillators

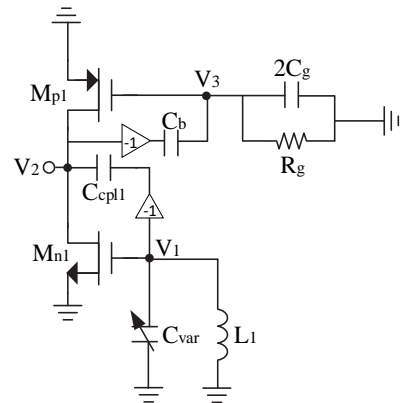


Figure 10. the half-circuit model of the proposed oscillator

4. SIMULATION RESULTS

Figure 11 shows the time domain of the differential output waveform of the proposed structure which designed in 0.18 μm TSMC CMOS technology with 1.8 v supply voltage for 900 MHz output frequency. $\frac{w}{L}$ of

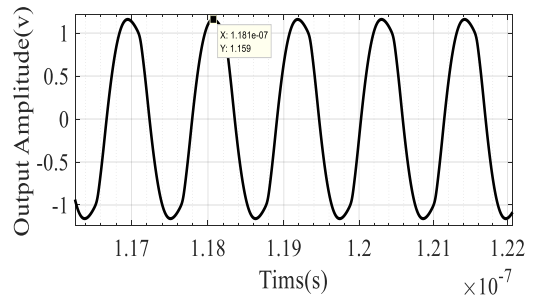


Figure 11. Time-domain of the output waveform for the proposed oscillator

the NMOS transistor is 320 and $\frac{w}{L}$ of The PMOS transistor is 160. Phase noise for the proposed oscillator at 1MHz offset frequency is -138.4 dBc/Hz . The proposed oscillator in this work and the mentioned oscillator in literature [6] are simulated in the same condition. Table 2 summarizes the phase noise, and FOM for both mentioned oscillators in 100 kHz, 1 MHz, and 10 MHz offset frequencies. FOM is calculated by Equation (6) [8].

$$FOM = 10 \log \left(\frac{\omega_0}{\Delta\omega} \right)^2 \frac{1}{P.L(\Delta\omega)} \quad (6)$$

In which, ω_0 , $\Delta\omega$, $L(\Delta\omega)$, and P are the oscillation frequency, offset frequency, phase noise at $\Delta\omega$ and power consumption, respectively. Table 3 presents a performance summary of the proposed oscillator compared with some previously published oscillator designs.

TABLE 2. Performance comparison of both mentioned structures

Offset frequency	Osc. of Figure 1			Proposed Osc. of Figure 4		
	@100 kHz	@1MHz	@10MHz	@100 kHz	@1MHz	@10MHz
Phase noise (dBc/Hz)	-110.2	-132	-152.3	-114.5	-138.4	-160
FOM(dB)	-212.48	-214.48	-214.78	-216.04	-219.94	-221.54

TABLE 3. Performance summary of the proposed structure and comparison with previously published design

Technology nm	FOM dB	Phase noise dBc/Hz	Freq. GHz	Power mw	VDD V	Ref Unit
180	-216@1MHz	-125@1MHz	1.75	2.3	1.8	[8]
180	-218.8@1MHz	-116.8@1MHz	4	1	1.8	[9]
180	-215.6@3MHz	-136@3MHz	2.4	7	1.8	[10]
180	-217.4@1MHz	-130.3@1MHz	1.8	6.3	1.8	[11]
180	-215.8@1MHz	-122.8@1MHz	2.55	3.2	1.2	[12]
180	-211@1MHz	-116.6@1MHz	2.89	2.86	1.8	[13]
180	-213.8@1MHz	-113.6@1MHz	4.35	1.8	1.4	[14]
180	-219.4@1MHz	-141.5@1MHz	0.9	12.87	1.8	[15]
180	-211.1@1MHz	-120.3@1MHz	4	13.21	1.8	[16]
180	-220@1MHz	-138.4@1MHz	0.9	5.59	1.8	This work

5. CONCLUSION

We found that the zero-crossings points have a major effect on total phase noise using the concept of ISF in Hajimiri's phase noise model. The operation points of the transistors effect on the ISF at zero-crossings points. We show the low loop gain at these moments reduces ISF significantly. Based on these investigations, a novel circuit technique for phase noise reduction in LC cross-coupled oscillators was proposed in the paper. The proposed structure changes the operation region in the zero-crossings point. This alteration reduces the closed-loop gain at this moment and moves the high loop gain at a lower sensitive phase than zero-crossings points. In comparison with the original structure, the proposed oscillator improved the phase noise and FOM, about 6.4 dB and 5.5 dB, respectively.

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Persian Abstract

چکیده

در این مقاله یک تحلیل بصری روی یکی از تکنیک‌های کاهش نویز فاز انجام شده است و سرانجام یک ساختار بهبود یافته از نظر عملکرد نویز فاز معرفی شده است که از نمونه‌ی پیشین خود نویز فاز بهتری دارد. این تکنیک اثر منابع نویز را در نقاط گذر از صفر با استفاده از کاهش بهره‌ی حلقه بسته کم می‌کند. پیش از این بهره‌ی حلقه بسته در این ساختار در نقطه‌ی گذر از صفر بیشینه بود که با استفاده از این تکنیک این مقدار بیشینه به نقطه‌ای دورتر از نقطه‌ی گذر از صفر منتقل شده است. این کاهش بهره با استفاده از ضرایب متفاوتی مورد آزمایش قرار گرفت که همگی بهبود عملکرد نویز فاز را نشان دادند. در واقع این روش نویز فاز را با دست‌کاری نواحی کاری ترانزیستورها بهبود می‌دهد. تابع حساسیت ضربه (ISF) به روشنی بهبود نویز فاز را در ساختار طراحی شده‌ی هدف در مقایسه با ساختار پیشین نشان می‌دهد. ما نوسان ساز هدف را با استفاده از فناوری استاندارد 0.18 CMOS TSMC طراحی کرده‌ایم. نوسان ساز هدف در فرکانس 900 مگاهرتز با جریان مصرفی 3.11mA و ولتاژ تغذیه 1.8v طراحی شده است که با این طراحی نویز فاز مقدار -138.4 dBc/Hz دارد.
