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A Simple General-purpose I-V Model for All Operating Modes of Deep Submicron MOSFETs

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ABSTRACT

A simple general-purpose I-V model for all operating modes of deep-submicron MOSFETs is presented. Considering the most dominant short channel effects with simple equations including few parameters, a reasonable trade-off between simplicity and accuracy is established. To further improve the accuracy, model parameters are optimized over various channel widths and full ranges of operating voltages using a heuristic optimization algorithm. The obtained results demonstrate only 1.28% and 0.97% average error in IBM 0.13um CMOS technology node for NMOS and PMOS, respectively, comparing with the accurate physically-based BSIM3 model. Furthermore, the tolerance of the model accuracy against parameters variation is investigated.

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1. INTRODUCTION

Modeling transistors I-V characteristics is an essential of any circuit design, both for intuitive analysis on paper and also for design verification in circuit simulators. The well-known square law model fails to represent the I-V behavior of submicron MOSFETs, because of ignoring short channel effects especially the velocity saturation and mobility degradation. Therewith, many different models have been proposed for submicron regimes [1-6], which can be generally divided into two groups. a) Models [1, 2, 6] which take the accuracy as the foremost priority and sacrifice simplicity for this sake, like BSIM3 [2], i.e. suitable to be implemented in circuit simulators such as HSPICE [7]. These models focus on emulating the physical behavior of MOSFETs very accurately and continuously, hence, they are complex and incorporate a large number of parameters. b) The other group of models [3-5, 8, 9] mainly focus on fast analysis while providing a reasonable accuracy. To set a balance between simplicity and accuracy, they try to keep the complexity as low as an acceptable accuracy. In this sense, such models usually entail few parameters incorporated in tractable equations. An efficient model of this type known as alpha-power law, proposed by Sakurai and Newton [4], is an expansion of square-law. This model includes the velocity saturation effect in short channel MOSFETs, but suffers from some main shortcomings. First, the saturation drain current and the saturation drain-source voltage are size dependent, second, the drain current in linear mode is related to the drain-source voltage linearly which is a considerable source of inaccuracy, last but not the least, the model does not consider the channel length modulation effect on the drain current which is very effective especially as the channel length shrinks. A while after, the authors introduced the n^{th}-power law model [5], a modified version of the previously proposed model, to overcome the above shortcomings. However, the accuracy of the initial n^{th}-power law model deteriorates in deep submicron devices, mainly because it ignores the mobility degradation, threshold voltage variations due to scaling and Drain Induced Barrier Lowering (DIBL), and the sub-threshold current, whose impacts on the transistor I-V behavior are critical especially in deep submicron regimes. Several models

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[8-11], which are further discussed in section 2, tried to modify the initial n[th]-power law model to fit the characteristics of nanometer devices. This is quite a challenging task, since various complex phenomena influence the drain current in deep submicron devices [2]. To achieve a reasonable trade-off between simplicity and accuracy, the most dominant phenomena should be considered and approximated by simple equations and few parameters as possible. On the other hand, setting proper values to parameters is a deciding factor on the overall accuracy of the model. The parameters values should be globally optimum for full ranges of operating voltages and various channel widths. I-V equations of submicron MOSFETs are highly nonlinear, have two separate relations for linear and saturation sections, and involve at least several parameters. In such conditions, the classic gradient-base optimization methods [8] usually stuck in local extrema, and their performance highly depends on the initial guess. On the other hand, heuristic optimization methods can efficiently find the global optimum for such complex multi-variable problems without requiring carefully set initial values.

Totally, the previous modifications made on n[th]-power law model suffer from one or more drawbacks: not setting a reasonable trade-off between simplicity and accuracy i.e. overcomplicating the equations or adding too many extra parameters for sake of accuracy [9], designed for a special purpose like delay analysis or just applicable in digital circuits [6, 12, 13], not covering all operating modes [8, 9], and not applying a fast efficient optimization algorithm [8, 11]. Regarding the existing gaps, this paper presents an I-V model for deep submicron MOSFETs with the following main features:

- A well-established simplicity-accuracy trade off

The model takes into account the most dominant short channel effects through all operating modes (sub-threshold, triode, and saturation) by simple equations and few added parameters. The accuracy is further improved by optimizing the model parameters across various channel widths and full ranges of operating voltages. Furthermore, the tolerance of accuracy against each parameter variation is investigated.

- General-purpose

  The model is not designed for any special application. It can be used in both analog and digital circuits for any purpose where the I-V model has to be applied.

- Heuristic optimization algorithm

  The model parameters are optimized by a heuristic method, which can efficiently find the global optimum of such a nonlinear complex problem. Heuristic algorithms start from a random initial population and do not require a carefully selected initial point [14, 15]. They are fast and do not impose heavy computational loads on the overall system. The applied heuristic method, named Artificial Bee Colony (ABC) [16], has only three control parameters, so it is easily configurable [17, 18].

The obtained results demonstrate only 1.28% and 0.97% error in IBM 0.13um CMOS technology node for NMOS and PMOS, respectively, comparing with the accurate physically based model of BSIM3. The rest of the paper is organized as follow. Section 2 reviews some similar models. Section 3 explains the proposed model and the optimization process. Section 4 contains the simulation results. Finally, Section 5 concludes the paper.

2. REVIEW of SOME SIMILAR MODELS

The initial n[th]-power law model [5] was introduced as follow.

In linear mode, $V_{DS} \le V_{DSsat}$

$$I_D = I_{Dsat}(2\frac{V_{DS}}{V_{DSsat}} - \frac{V_{DS}^2}{V_{DSsat}^2})(1+\lambda V_{DS}), \quad (1)$$

in saturation mode, $V_{DS} > V_{DSsat}$

$$I_D = I_{Dsat}(1+\lambda V_{DS}), \quad (2)$$

where

$$I_{Dsat} = \frac{W_e}{L_e} B(V_{GS} - V_t)^n, \quad (3)$$

$$L_e = L + XL - 2L_D, \quad (4)$$

$$W_e = W + XW - 2W_D, \quad (5)$$

$$\lambda = \lambda_0 + \lambda_1 V_{SB}, \quad (6)$$

$$V_{DSsat} = K(V_{GS} - V_t)^m, \quad (7)$$

$$V_t = V_{t0} + \gamma(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}). \quad (8)$$

V_{DS} , V_{GS} , and V_{SB} are the drain-source, gate-source and source-bulk voltages, respectively. V_{DSsat} is the drain-source voltage at which the average carrier drift velocity saturates. W_e and L_e are the effective channel width and length, respectively. L and W are the drawn channel length and width, respectively. XL and XW are models masking and etching effects on gate length and width, respectively. L_D is the lateral diffusion into the channel from the source/drain diffusion mode, W_D is the sideway diffusion into the

channel from the bulk along the width, Φ_F is the potential difference between the electrostatic potential and the Fermi potential inside the substrate under thermal equilibrium, and V_{t0} is the threshold voltage at $V_{SB}=0$. B is a technology dependent constant, which implicitly includes mobility. γ is the body-effect coefficient. λ_0 is the channel length modulation coefficient at $V_{SB}=0$. n, m, K, and λ_1 are empirical constants. Therefore, at $V_{SB}=0$, the six parameters of initial n[th]-power law are $[V_{t0}, B, \lambda_0, K, m, n]$. As mentioned before, the initial n[th]-power law assumes mobility (included in B) and V_t constants over all V_{DS} and V_{GS} which leads to a considerable inaccuracy in submicron regimes. Furthermore, the sub-threshold current is not taken into account. Hamoui [8] considered the effects of short channel length and width on V_{t0} as follows:

$$V_{t0}=V_{tw}(1+f\frac{L_e}{W_e}), \tag{9}$$

where V_{tw} is the threshold voltage of wide channel MOSFETs at $V_{SB}=0$ and f is an empirical factor. He modified the model with seven parameters at $V_{SB}=0$ as $[V_{t0}, f, B, \lambda, K, m, n]$. Hamoui claimed that the DIBL effect was implicitly considered in his proposed modified model, as the threshold voltage would be optimized over the full range of V_{DS} voltage. However, the model is not accurate enough in deep submicron regimes. Since, just optimizing the threshold voltage over V_{DS} cannot sufficiently model the DIBL effect on V_{t0}. The mobility is not constant over all V_{GS}. Addressing the sub-threshold current just by optimizing V_{tw} is quite insufficient. Finally, a classic gradient-base optimization method would easily stick in local extrema.

The authors in [9, 11] considered the mobility degradation and hence rewrote B as $B=B_0\mu$. B_0 is a constant and the hole and electron mobility were empirically approximated as $\mu_{hole}=k/B_0(1+\beta V_{DS})^2$ and $\mu_{elec}=k/B_0(1+(\beta V_{DS})^2)^{3/2}$, respectively. Where $\beta=\mu_0/(L_eV_{sat})$ and $k=B_0\mu_0/L_e$. μ_0 is the carrier mobility and V_{sat} is the voltage at which the carrier velocity saturates. The dominant effect of V_{GS} on mobility degradation was not accounted [2]. The authors also applied the empirical equation $\lambda=\lambda_C/\sqrt{1+\lambda_V V_{DS}}$ which models the variations of λ with V_{DS} [19], where λ_C and λ_V are constants. An empirical relation to model the variation of the threshold voltage due to the DIBL effect was used as follows:

$$\Delta V_t=\frac{-\sigma\sqrt{V_{DSsat}}V_{DS}}{L_e}, \tag{10}$$

where σ is a constant. The effects of short channel length and width were ignored while they are crucial in deep submicron devices. The authors also suggested $W_e=W-(W_W/W)-(W_{VGS}/V_{GS})$, where W_W and W_{VGS} are constants. The authors introduced the following equation for drain current in deep inversion:

$$I_D=I_{Dsat}(1+\lambda V_{DS})^p. \tag{11}$$

while around V_{DSsat}, the drain current was computed as follow:

$$I_D=I_{Dsat}(2-\frac{V_{DS}}{V_{DSsat}})^q\frac{V_{DS}}{V_{DSsat}}(1+\lambda V_{DS}). \tag{12}$$

As it is obvious, p and q added extra degrees of nonlinearity to the overall model. They considered thirteen parameters at $V_{SB}=0$ in their modified model as $[V_{t0}, K, m, n, \lambda_C, \lambda_V, \sigma, \beta, k, W_W, W_{VGS}, p, q]$ and applied a two-stage optimization process where first the most effective parameters were selected by the genetic algorithm and then just the selected parameters were optimized by simulated annealing method i.e. a huge optimization process imposing a heavy computational load. In addition, to weak points of the model, stated above, the sub-threshold current is not considered.

The author in reference [10] claimed that the proposed model to work both in moderate and inversion modes:

$$I_{Dsat}=\begin{cases} I_0 e^{\frac{V_{GS}-V_t}{N_S}}, & V_{GS}<V_{Th} \\ I_0 e^{\alpha}(\frac{V_{GS}-V_t}{N_S})^{\alpha}, & V_{GS}\geq V_{Th} \end{cases}, \tag{13}$$

where $V_{Th}=V_t+\alpha N_S$. This modified model incorporates seven parameters at $V_{SB}=0$ as $[V_{t0}, I_0, \alpha, N_S, K, m, n]$. The sub-threshold current, variations of V_t due to channel width and length and the DIBL effect, and the effect of channel width and length on I_{Dsat} were ignored.

Another modified n[th]-power law model in saturation mode [12] was proposed as $I_D=I_{Dsat}(1+\lambda_m V_{DS})(1-d(V_{GS}-1))$, where $\lambda_m=(aV_{GS}^b+C)+\lambda_1 V_{SB}$ and $I_{Dsat}=B(V_{GS}-V_t)^n-\delta(W_e/V_{GS}^{1+n})$. No optimization process was applied and the parameters were extracted from BSIM4 or the same manner as [5]. This modified model incorporated ten parameters at $V_{SB}=0$ as $[V_{t0}, B, a, b, c, d, \delta, K, m, n]$. Mobility

degradation and variations of threshold voltage, and the sub-threshold current were ignored.

3. THE PROPOSED MODEL

Regarding the existing weak points of the similar models, discussed in details in the previous section, the proposed model takes into account the most dominant short channel effects on the drain current. These effects include the mobility degradation, threshold voltage variations due to scaling and DIBL effect, and sub-threshold current. For $V_{GS} > V_t$ a modified version of n^{th}-power law is proposed. However, since n^{th}-power law is not able to model weak inversion especially in deep submicron regimes, a simple equation is added to account for the sub-threshold current. The model parameters are optimized over full ranges of V_{GS} and V_{DS}. Considering the dominant short channel effects along with parameter optimization over full ranges of operating voltages result in an accurate enough model across all operating modes. The details of the proposed model are explained as follow.

3. 1. Mobility Degradation To account for the mobility degradation effect, B is written as $B = B_0\mu$, where B_0 is a constant. The mobility is modeled, by considering the most dominant cause of its degradation i.e. V_{GS} [2], just by adding one extra parameter (μ_1) as follows:

$$\mu = \frac{\mu_0}{1+\mu_1 V_{GS}}. \tag{14}$$

3. 2. Modified Threshold Voltage The most dominant short channel effects on threshold voltage are: increasing as channel length shrinks, increasing as channel width narrows, and decreasing by V_{DS} (DIBL), all of which are considered [8, 20], just by adding two extra parameters of σ and f as follows:

$$V_{t0} = (V_{tw} - \sigma V_{DS})(1 + f\frac{L_e}{W_e}), \tag{15}$$

where V_{tw} is the threshold voltage of a long channel device at $V_{SB} = 0$.

3. 3. Sub-threshold Current The sub-threshold current of MOSFET is critical, especially in deep submicron regimes. It cannot be modeled just by optimizing parameters of the modified n^{th}-power law model in sub-threshold mode, but has to be modeled separately. Some models of the sub-threshold current are complex, absolutely accurate, but not suitable for intuitive analysis [6], and some are simple but not accurate enough because of ignoring dominant effects like exponential variations by V_{DS} [21] or not optimizing the parameters over full ranges of operating voltages [22]. The proposed equation for the sub-threshold current, inspired from BSIM3 [2], is as follows:

$$I_{Dsub} = I_0(1 - e^{-\frac{V_{DS}}{n_{sub}V_T}})e^{\frac{V_{GS}-V_t-V_{OFF}}{n_{sub}V_T}}(1+\beta V_{DS}), \tag{16}$$

where $1 < n_{sub} < 3$, V_T is the thermal voltage as KT/q, V_{OFF} is a negative offset voltage to compensate for the threshold voltage difference in the sub-threshold mode, β is a constant proposed in this work to model the linear dependence of I_{Dsub} on V_{DS}, and I_0 is considered as follows:

$$I_0 = \alpha\mu\frac{W_e}{L_e}\sqrt{\frac{q\varepsilon_{si}N_{CH}}{4\phi_B}}V_T^2, \tag{17}$$

where α is a constant proposed here to modify I_0 for deep submicron devices, and other constants are defined the same as reference [2]. The proposed model incorporates nine parameters as $[V_{tw}, f, \sigma, B_0, \mu_1, \lambda_0, K, m, n]$ at $V_{SB} = 0$ in the above threshold mode, and four parameters as $[\alpha, n_{sub}, V_{OFF}, \beta]$ in the sub-threshold mode. Therefore, the proposed model works in all operating modes with a reasonable accuracy just by thirteen parameters.

3. 4. Optimization Process The MOSFET I-V models entail nonlinear equations involving at least several parameters, whose number grows as the channel length shrinks. Therefore, applying classic optimization methods for extracting model parameters usually results in local extrema. Heuristic optimization algorithms are efficient alternatives. The Artificial Bee Colony method is a heuristic swarm-based algorithm, proposed by Karaboga at 2005 [16] inspired from foraging behavior of honey bees. The ABC optimization algorithm best suits multi-variable continuous optimization problems, and has only three controlling parameters, hence, it is easy to configure. The following steps are repeated in the ABC algorithm until a stopping criterion is met.

- Step 1: Initial Phase

A random population from the search space is formed by the following equation:

$$X_{mi} = X_i^{\min} + rand \times (X_i^{\max} - X_i^{\min}),$$
$$m = 1, 2, ..., SN \text{ and } i = 1, 2, ..., n \tag{18}$$

where X_{mi} is a solution vector, SN is the total population size or the total number of solution vectors, $X_i^{\min}$ and $X_i^{\max}$ are n-dimensional vectors specifying

respectively the lower and upper range of solution vector, and rand is a random number between [0,1]. The fitness of each solution is then computed.

- Step 2: employed bee phase

A new solution is produced in the neighborhood of X_{mi}:

$$V_{mi} = X_{mi} + \phi_{mi}(X_{mi} - X_{ki}), \tag{19}$$

$$k = \text{int}(rand \times SN) + 1. \tag{20}$$

ϕ_{mi} is the a monotonic distribution of real random numbers between $[-1,1]$. As can be seen from Equation (20), k is chosen randomly among $\{1,2,...,SN\}$. The new solution replaces the previous one only if it has a better fitness.

- Step 3: Onlooker Bees Phase

In this phase, a solution is selected according to its probability amount (P_m) calculated as follows by applying a selection method like Roulette Wheel:

$$P_m = \frac{fit_m(X_m)}{\sum_{m=1}^{SN} fit_m(X_m)}, \tag{21}$$

where $fit_m(X_m)$ is the fitness of solution X_m. The number of selected solution equals SN. Then, step 2 is repeated again in the present step. All three steps iterate until a stopping criterion is met. If a solution is not improved after a predetermined number of iterations (limit), that solution is discarded and a new one is produced randomly as step 1.

The model parameters are optimized applying the following fitness function:

$$E = \frac{1}{N_{VGS}.N_{VDS}.N_W} \sum_{N_{VGS}} \sum_{N_W} \sum_{N_{VDS}} \left(\frac{I_{Dmeasured} - I_{D\,model}}{I_{Dmeasured}}\right)^2, \tag{22}$$

where N_{VGS}, N_{VDS}, and N_W are, respectively, the number of V_{GS}, V_{DS}, and channel widths points. $I_{Dmeasured}$ is the accurate drain current obtained from BSIM3 model, while $I_{D\,model}$ is the drain current calculated by the proposed model.

4. SIMULATION RESULTS

To examine the accuracy of the proposed model, the obtained results were compared with the results of an accurate physically based method (BSIM3). To insure the efficiency of the model over different device sizes including narrow width channels, various widths between $W = 1L$ to $W = 5L$ were considered, where $L = 0.13um$. The model parameters are optimized through full ranges of V_{GS} and V_{DS} i.e. $[0,1.3V]$. The values of model parameters for NMOS/PMOS are reported in Table 1.

TABLE 1. NMOS/PMOS parameters values

above threshold			sub-threshold		
parameters	**NMOS**	**PMOS**	**parameters**	**NMOS**	**PMOS**
$\|V_{tw}\|$	0.3899	0.4233	m	0.7394	0.7821
f	0.0421	0.0388	n	1.7488	1.6457
σ	0.0785	0.0120	α	0.4460	0.4720
B_0	0.3606	0.2915	n_{sub}	1.4361	1.4038
μ_1	0.8900	0.0560	V_{OFF}	-0.0690	-0.0893
λ_0	1.0000	0.1736	β	1.0000	0.0000
K	0.3269	0.6557			

The optimization algorithm efficiently converged to the global minimum of the error function in Equation (22), over various channel widths and the full ranges of operating voltages, after about 200 iterations (as depicted in Figure 1). For both NMOS and PMOS devices, the population size was 200 and the value of limit parameter was 100. The average error was 1.28% and 0.97% for NMOS and PMOS, respectively over entire operating modes (sub-threshold, triode, and saturation). In order to demonstrate the accuracy of the proposed model, Figure 2 shows how precisely the drain current computed by the proposed model fits the exact current obtained from BSIM3 model. Since the current scaling in sub-threshold and above threshold modes are different, these two modes are depicted in separate figures for a better resolution.

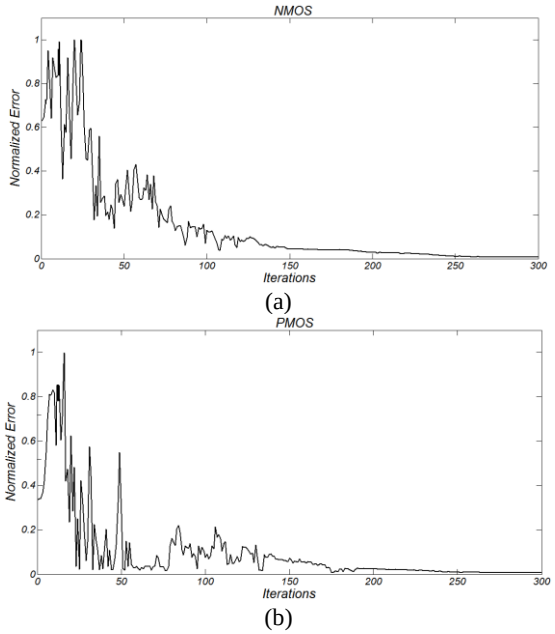


Figure 1. The convergence of normalized error function for a) NMOS b) PMOS

The average error in the sub-threshold mode is 2.31 and 1.76% for NMOS and PMOS respectively, while in the above threshold it is 0.86 and 0.45%. As it is obvious from parameters values in Table 1, Figure 2, and Figure 3, the linear dependence of NMOS drain current on V_{DS} is stronger than that of PMOS in both sub-threshold and above threshold modes.

Table 2 compares the proposed model with some other similar models and the accurate model of BSIM3 in terms of simplicity, accuracy, and generalization. As can be concluded from the table, considering the technology node, number of parameters, and equations simplicity, the proposed model establishes a robust trade-off of simplicity-accuracy and also is applicable in all operating modes for any purpose.

The number of parameters and the reported error for the proposed model are for entire operating modes. None of the reported similar models are applicable in the sub-threshold mode, while the proposed model covers all operating modes with a comparable number of parameters, simpler equations, and a better overall accuracy for both NMOS and PMOS devices.

To explain the robustness of the proposed model against parameters variations and to recognize the most sensitive parameters, the tolerance of the error function in Equation (22) is computed as follows:

$$Error\_Tolerance = \frac{E_{dev} - E_{opt}}{E_{opt}}, \quad (23)$$

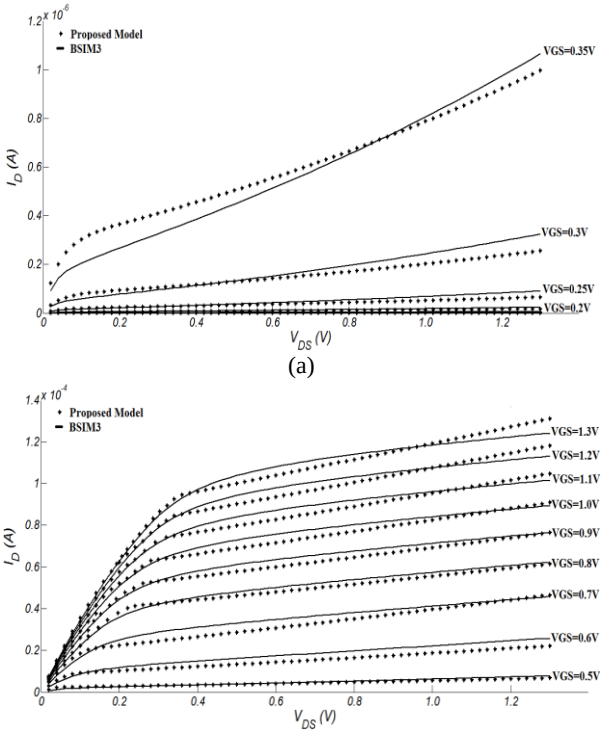
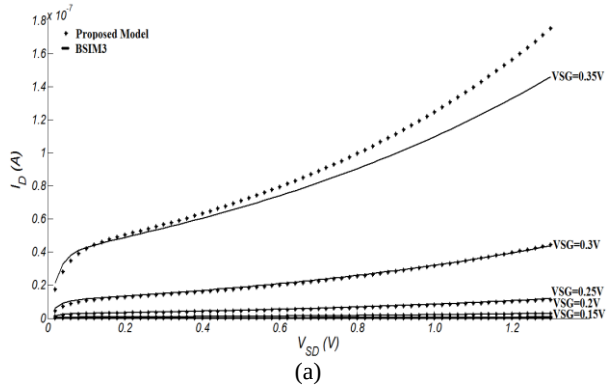


Figure 2. NMOS I-V characteristic a) sub-threshold mode b) above threshold mode

TABLE 2: Comparisons with some similar models

Ref.	Technology Node nm	No. of Param.	Simplicity	Op. Modes			Average Error%	
				Sub.	triode	Sat.	NMOS	PMOS
[5]	250	6	good	×	✓	✓	3.7	7.5
[8]	800	7	good	×	✓	✓	6	6
[9]	180	13	poor	×	✓	✓	1.3	3.1
[10]	360	7	medium	×	✓	✓	2-3	2-3
[12]	90	10	medium	×	✓	✓	1.33	N/A
BSIM3	-	100	complex	✓	✓	✓	0	0
This work	130	13	good	✓	✓	✓	1.28	0.97



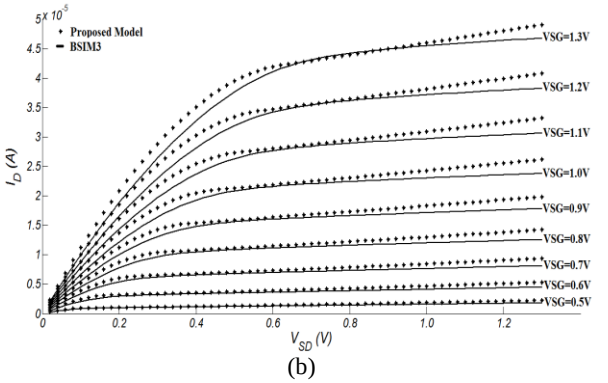


Figure 3. PMOS I-V characteristic a) sub-threshold mode b) above threshold mode

where E_{dev} is the deviated error from the optimum error E_{opt}, because of parameters variations.

The amount of error tolerance caused by %10 variation of each parameter from its optimum value is reported in Table 3. As expected, the most sensitive parameter is the threshold voltage which is effective in all operating modes, hence its unsuitable setting leads to a considerable source of error. Most of other parameters cause less than %10 percent variations in error tolerance by changing up to %10 percent. Figure 4 shows the error tolerance caused by the variation of a sample parameter (λ_0).

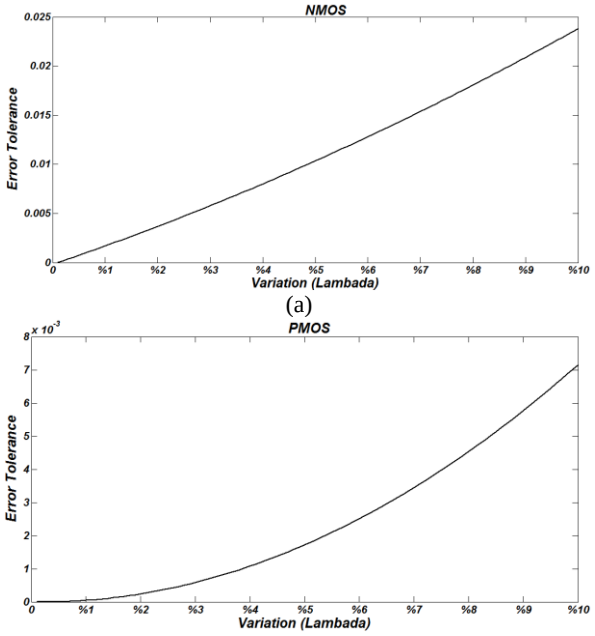


Figure 4. Error tolerance of the model with variations of λ_0 a) NMOS b) PMOS

TABLE 3. Error tolerance (%) with 10% variations of parameters

Above threshold			sub threshold		
parameters	**NMOS**	**PMOS**	**parameters**	**NMOS**	**PMOS**
V_{tw}	50.52	48.03	m	1.8	1.59
f	0.47	0.32	n	13.6	13.30
σ	4.40	4.22	α	6.80	6.48
λ_0	2.38	0.72	n_{sub}	15.90	14.30
μ_1	0.13	0.05	V_{OFF}	10.21	9.55
B_0	6.32	6.14	β	4.00	0.00
K	3.73	3.62			

5. CONCLUSIONS

A simple general-purpose I-V model for all operating modes of deep submicron MOSFETs was presented. The proposed model addressed weak points of other similar models by considering dominant short channel effects such as the mobility degradation, threshold voltage variations due to scaling and DIBL effect, and the sub-threshold current. Considering the dominant short channel effects approximated by simple equations and a reasonable number of parameters along with parameters optimization over various device sizes and full ranges of operating voltages balanced the trade-off between accuracy and simplicity robustly in all operating modes. The proposed model demonstrates only 1.28% and 0.97% average error in IBM 0.13um CMOS technology node for NMOS and PMOS, respectively, comparing with the accurate physically based model of BSIM3. Furthermore, the tolerance of accuracy against each parameter variation was investigated, which indicated the robustness of the proposed model against parameters variations.

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A Simple General-purpose I-V Model for All Operating Modes of Deep Submicron MOSFETs

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چکیده

مدل جریان–ولتاژ همه منظوره ساده‌ای برای تمامی نواحی کاری ترانزیستورهای ماسفت زیرمیکرون عمیق ارائه می‌شود. با در نظر گرفتن موثرترین اثرات کانال کوتاه در قالب معادلاتی ساده شامل تعداد کمی پارامتر، مصالحه‌ای منطقی میان سادگی و دقت یافته است. جهت بهبود بیشتر دقت، پارامترهای مدل روی عرض‌های کانال مختلف و محدوده‌های کامل ولتاژهای کاری با استفاده از الگوریتم بهینه‌سازی ابتکاری بهینه شده‌اند. نتایج به دست آمده تنها خطای متوسط ۱٫۲۸٪ و ۰٫۹۷٪ را در تکنولوژی IBM 0.13um CMOS به ترتیب برای NMOS و PMOS، در مقایسه با مدل فیزیکی دقیق BSIM3 نشان می‌دهند. به علاوه، انحراف دقت مدل نسبت به تغییرات پارامتر بررسی شده است.

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