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Design of Arrayed Waveguide Grating based Optical Switch for High Speed Optical Networks

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ABSTRACT

This paper demonstrates the design of an Arrayed Waveguide Gratings (AWG) based optical switch. In the design both physical and network layer analysis is performed. The physical layer power and noise analysis is done to obtain Bit Error Rate (BER). This has been found that at the higher bit rates, BER is not affected with number of buffer modules. Network layer analysis is done to obtain performance in terms of packet loss rate and average delay. Analysis presented in the paper clearly reveals that there is a minimum amount of power required, which is necessary for the satisfactory performance of switch both at physical and network layer.

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1. INTRODUCTION

For the present internet communication infrastructure optical network is becoming an important aspect due to the huge bandwidth provided by the optical fiber. Optical fiber cables are used today for more than 80 percent of the world's long-distance communication. It is envisaged that, in all-optical network, buffering, switching and routing within the network nodes will be performed optically; while traffic at the backbone network will remain in optical domain. Network elements such as optical add/drop multiplexers and optical cross-connects will have full control on all wavelengths. They are expected to have full knowledge of the status of each wavelength and the traffic carrying capacity [1-4]. The main problem in such all-optical network is the unavailability of optical RAM and technology is not matured for optical processing.

Packet switching is an appropriate switching technique in all-optical network rather than circuit switching because of inefficient bandwidth utilization and is less costly in maintaining a circuit. Different contention resolution techniques are proposed which try to resolve contention.

Optical buffers combining with tunable wavelength converters (TWCs), fiber delay lines can solve bottlenecks in limitations of optical switching.

The performance evaluation of the switches can be done both at physical as well as network layer [5-8]. Physical layer analysis is crucial in designing the basic parameters like switch size and buffering conditions. Parameter like packet loss probability is used to measure performance of the switch in network layer. For efficient switching high throughput is desired therefore low packet loss probability is to be achieved. In the physical layer, effects of system impairment on bit-error rate (BER) are studied.

Physical layer impairments are dominated by amplified spontaneous emission (ASE) noise and crosstalk, which also leads to packet drop. In this paper, we estimate the performance characteristic of buffer modules which are key elements of optical data centers. We also discuss the design of an improved version of AWG based optical packets switch along with power budget analysis. The detailed analysis shows that the architecture presented here can operate in the sub-micro watts in comparison to the earlier optical switch which operates in milli-watts regime [9].

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2. RELATED WORK

Optical packet switch is considered as viable options for high speed data transfer and in optical data centers. For realizing on demand high bandwidth connectivity between top of rack switches; Proteus [10, 11] uses wavelength selective switch modules and optical circuit switches. For designing large switch matrix, Petabit [12] uses low radix AWG routers and tunable wavelength convertors. In the recent development [13, 14], Hy Scale (hybrid optical network based scalable switch centric architectures) is a switch centric recursively defined network that uses both optical burst switching and optical circuit switching. The switch proposed in [15] is a high speed switch, which uses TWCs and AWG to switch packets optically while buffering contending packets in a single shared electronic buffer.

In previous research ye et al. [16] performs a comparison between single wavelength fiber delay lines and electronic buffer in the context of AWG switch. In [9, 17-20], AWG based optical switch architectures are proposed with various buffer and SOA placements combinations. In [21], a hybrid optical/electronic buffering scheme and a method for efficiently integrating fiber delay line buffer capacity into the AWG wavelength assignment scheme. However, in this design O/E and E/O conversion is necessary to write and readout of the packets and may be good for data centres but not for optical switching.

In the similar directions, H. Rastegarfar [22] proposed a switch in which recirculating FDLs are used for storing the contending packets. In the switch, the packets which feel contention are directed towards recirculating FDL ports for buffering and when the contention is resolved then these packets are forwarded in the direction of output port fiber.

This switch has number of limitations which some of them are discussed as below:

- The main advantage of WDM is lost; here by using the routing pattern of AWG N=32 packets can be stored in a single piece of fiber.
- The another major limitation of switch is that the switch stores total of N packets in the buffer while on the other hand the proposed switch can stored, maximum of N^2 packets.
- In [23], authors also state that the packets remains in the buffer unit for single recirculation, then in such scenario what is the use of recirculating buffer?

This paper discusses an AWG based design. Power budget analysis is done, to evaluate the BER at the output of the switch under various power levels. This paper, also discusses how the, size of the packet and bit rate affects the BER performance of the switch. How the number of buffer modules affects the performance in terms of BER. To evaluate the performance of the switch at the network level, packet loss performance and average delay is performed, and results are compared with recently published design.

3. SWITCH DESIGN AND ANALYSIS

In the architecture (Figure 1), switch is divided in the scheduling and switching section. The scheduling section contains the TWCs, one 2N×2N AWG router, FDL lines for buffering of packets, and the switching section contains TWCs and an N×N AWG router [23]. The upper 'N' ports of scheduling AWG are connected to the 'N' FDL buffer modules. The other ports (N+1 to 2N) are actual input output ports. The input ports are equipped with the tunable wavelength converters (TWCs), and these TWCs are used to tune the wavelength of incoming packets as per the requirement of output packets. Suppose a packet arriving at input *'i'* and destined to the output *'j'* with required amount of delay of *'k'* time slots then the packet is routed to the k^{th} buffer module. To do so, the wavelength of the incoming packet is tuned as per the routing pattern of the cyclic AWG,

$$\lambda(i,k)=\lambda_l,\quad l=[1+(i+k-2)\bmod N] \tag{1}$$

The packet which is deflected through k^{th} buffer module will again re-appear after the delay of *'k'* time slots at the input port of scheduling AWG and due to the symmetric nature of scheduling AWG the packet get routed to the output port *'i'* of the scheduling AWG. Finally, the packet is forwarded towards the appropriate output *'j'* by tuning wavelength appropriately in the switching section.

3. 1. Physical Layer Analysis (Power Budget)

3. 1. 1. Power Analysis The loss in the power when packet passes through the switch is: $L_{TWC}L_{AWG}^{2N\times 2N}L_{FDL}L_{AWG}^{2N\times 2N}L_{TWC}L_{AWG}^{N\times N}$

To fully compensate the loss, the gain of the SOA placed at the input of the switching AWG must satisfy.

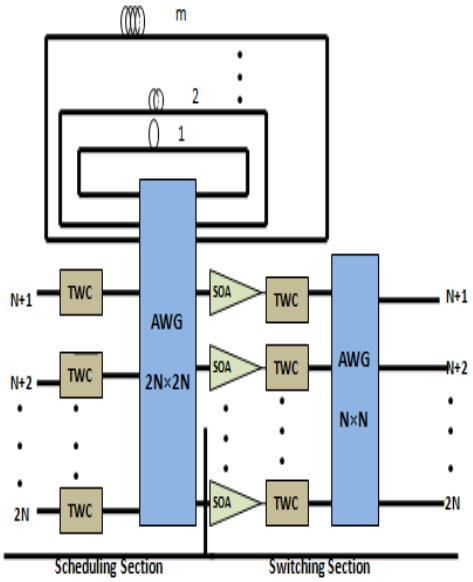

Figure 1. Design of AWG based Switch

$L_{TWC}L_{AWG}^{2N\times 2N}L_{FDL}L_{AWG}^{2N\times 2N}L_{TWC}L_{AWG}^{N\times N}G=1$

Power entering in the switch is:

$$P_s = bP_{in} \qquad b \in [0,1] \tag{2}$$

.The extinction ratio ($\varepsilon = P_0/P_1$) is assumed to be zero.

Power at the output of the switch is:

$$P_{out} = P_s + n_{sp}(G_3 - 1)h\nu B_0 L_{TWC} L_{AWG}^{N\times N} \tag{3}$$

3. 1. 2. Noise Analysis Various noise components are generated due to square law detection by the photo detector in the receiver. These noise components are ASE-ASE beat noise, shot noise, shot-ASE beat noise, sig-ASE beat noise, and thermal noise variances which are denoted by σ^2_s, $\sigma^2_{sp\text{-}sp}$, $\sigma^2_{sig\text{-}sp}$, $\sigma^2_{s\text{-}sp}$, and σ^2_{th} respectively [24]. The noises available at the receiver for a particular bit *b* are as follows:

Shot noise

$$\sigma_s^2 = 2qRPB_e$$

ASE-ASE beat noise

$$\sigma_{sp-sp}^2 = 2R^2 P_{sp}(2B_o - B_e)\frac{B_e}{B_0^2}$$

Sig-ASE beat noise

$$\sigma_{sig-sp}^2 = 4R^2 P \frac{P_{sp}B_e}{B_0}$$

Shot-ASE beat noise

$$\sigma_{s-sp}^2 = 2qRP_{sp}B_e$$

Thermal noise

$$\sigma_{th}^2 = \frac{4K_B T B_e}{R_L} \tag{4}$$

The expression for *P* and P_{sp} for TWC as a transparent device will be given by

$$P = bP_{in}$$

$$P_{sp} = n_{sp}(G_3 - 1)h\nu B_0 L_{TWC} L_{AWG}^{N\times N}$$

The total noise variance for bit b is:

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sp-sig}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2$$

$$BER = Q\left(\frac{I(1) - I(0)}{\sigma(1) + \sigma(0)}\right) \tag{5}$$

$$Q(z) = \frac{1}{\sqrt{2\pi}}\int_z^{\infty} e^{-\frac{z^2}{2}} dz \tag{6}$$

where, $I(1) = R\,P(1)$ and $I(0) = RP(0)$ are photocurrent sampled by receiver during bit 1 and bit 0 respectively, and *R* is responsivity of the receiver.

3. 1. 3. Power Budget Analysis Results In this section, results using above mathematical formulation are presented. Here, maximum allowed storage which is half of switch size is assumed, at various power levels. The available AWG routers can work well for 40 channels. In the analysis, we consider a 32×32 switch, as the size of the switch is of multiple of 2. The length of the loop is taken equal to the packet duration equivalent of slot duration and is given by [9].

$$L = \frac{cb_{it}}{nB_r} \tag{7}$$

Here, $c=3\times10^8$ m/s is the light speed, bit represents the total number of bits stored in FDL, (n =1.45) is the refractive index and Br represents the bit rate. Here, the Table 1 gives the values of all parameters used in the calculation.

As discussed in the previous section, the AWG is divided into two parts; first half port of AWG are connected with the FDL lines which are used for buffering purpose and the other half port of switch act as actual inputs and outputs. An AWG of size 32×32 is considered. In these 32 ports the first 16 ports will be used for the buffering of packets and other 16 ports are used as actual inputs/outputs.

In Table 2, results are tabulated for buffer size 16 and for different lengths of packets or time slots. Bit rate 10, 20 and 40 Gbps correspond to length of 19.3, 9.67 and 4.83 m, respectively. The length of fiber required here is small; considering loss of fiber to be 0.2 dB/Km, therefore the amount of loss will be less.

Hence, from above table, it can be concluded that for the proper operation of switch a power level of 2μW will be sufficient.

Considering power of 2μW, if the data rate is increased from 10 to 20 and 40 Gbps we see that BER reduces. Thus, as slot length decreases BER improves. The maximum data storage is not affected by the presence of crosstalk of AWG.

TABLE 1. List of Parameters [1]

Symbol	Parameter	Value
N	Size of the switch	16
n_{sp}	Population inversion factor	1.2
C	Speed of light	$3\times10^8 m/s$
N	Refractive index of fiber	1.45
R	Responsively	1.28 A/W
E	Electronic charge	$1.6\times10^{-19}C$
B_e	Electrical bandwidth	20GHz
B_0	Optical bandwidth	40GHz
L_{TWC}	TWC insertion loss	2.0 dB
$L_{AWG}^{2N\times 2N}$ $L_{AWG}^{N\times N}$	Loss of Scheduling and Switching AWG (32 channels)	3.0 dB
L_{FDL}	Loss of the fiber loop	0.2 dB/km

TABLE 2. BER analysis of switch at various power levels (buffer size =16, *b*=1000).

Power in μW	BER		
	B_r=10 Gbps	B_r=20 Gbps	B_r=40 Gbps
0.5	0.0027	0.0026	0.0025
0.6	9.6175×10^{-4}	9.2421×10^{-4}	9.0591×10^{-4}
1	1.7166×10^{-5}	1.6066×10^{-5}	1.5540×10^{-5}
2	8.4966×10^{-10}	7.4348×10^{-10}	6.9524×10^{-10}
3	4.4044×10^{-14}	3.6002×10^{-14}	3.2534×10^{-14}
4	2.2980×10^{-18}	1.7540×10^{-18}	1.5314×10^{-18}
5	1.1969×10^{-22}	8.5287×10^{-23}	7.1930×10^{-23}
6	6.2099×10^{-27}	4.1298×10^{-27}	3.3643×10^{-27}
7	3.2074×10^{-31}	1.9906×10^{-31}	1.5662×10^{-31}
8	1.6493×10^{-36}	9.5510×10^{-36}	7.2579×10^{-36}
9	8.4454×10^{-40}	4.5630×10^{-40}	3.3487×10^{-40}
10	4.3076×10^{-44}	2.1713×10^{-44}	1.5388×10^{-44}

So, as far as single switch is concern the crosstalk of AWG will not create any problem. In Table 3, BER analysis at power level of 2μW with number of modules is presented.

It is obvious from the table that as the number of modules increases, the BER also increases. Hence, if a power level of 2 μW is used then for a particular output only 10 packets can be stored, and then at the receiver, the BER will be under acceptable limit (≤10-9). Hence, all the 16 modules cannot be used if power level of 2 μW is used.

TABLE 3. BER analysis of switch at power levels of 2 μW varying number of modules (b=10000, bit rate = 40 Gbps).

Numbers of Modules	BER
16	1.2614×10^{-9}
15	1.2110×10^{-9}
14	1.1625×10^{-9}
13	1.1159×10^{-9}
12	1.0710×10^{-9}
11	1.0278×10^{-9}
10	9.8630×10^{-10}
9	9.4638×10^{-10}
8	9.0801×10^{-10}
7	8.7111×10^{-10}
6	8.3564×10^{-10}
5	8.0154×10^{-10}
4	7.6877×10^{-10}
3	7.3728×10^{-10}
2	7.0701×10^{-10}

Therefore, this analysis clearly reveals that in the designing of any switch the physical layer parameters should be taken into account. As the buffering capacity have deep impact on the packet loss performance, this analysis is presented in next section.

4. Simulation Modeling

For the network layer analysis, calculations are done for parameters packet loss probability and average delay. For this simulation, modeling is done in Matlab. The entire process is divided into 3 main steps:

- Generation of information: random information in form of packets is generated at various inputs which are to be transmitted at destination.
- Generation and destination assignment of information: For each packet generated the destination port is assigned randomly but with equal probability.
- Buffer management: According to rules buffer is either utilized, and if buffer is full the packet is dropped.

The entire process is run several times approximately 10^6 to find out near to practical values for packet loss and average delay. The simulation pattern is based on random number generation and known as Monte Carlo simulation. The flowchart for the above three process are shown in Figures 2, and 3.

The parameters in Figures 2 and 3 are as defined below:

- *R*= Number of request generated (packets)
- ρ= Load
- *S*= Slot for Simulation
- *Y*= Random number

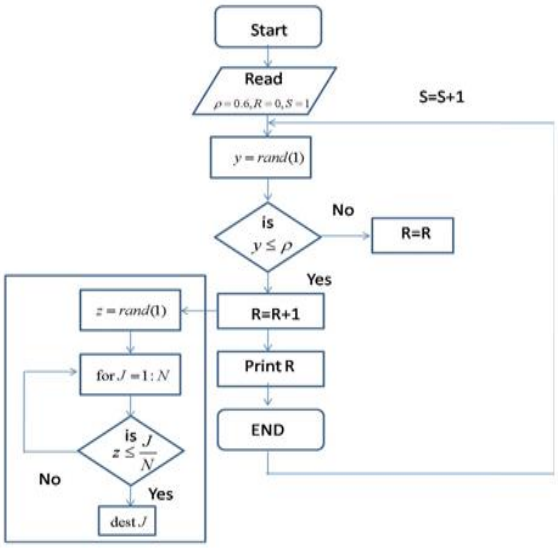

Figure 2. Generation and destination assignment of information

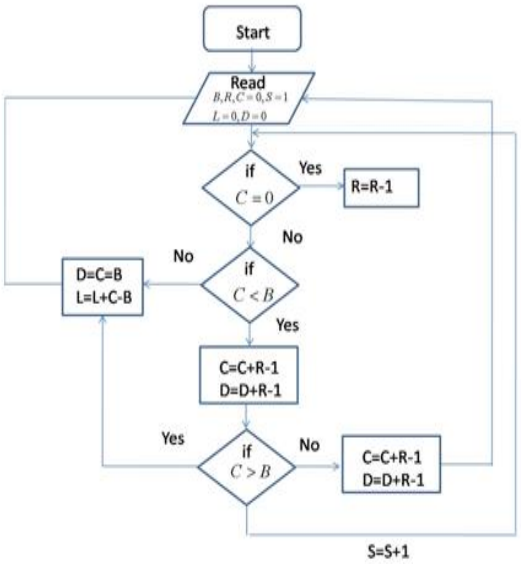

Figure 3. Buffer management

- *J*= Assigned Destination
- *L*=Loss
- *B*=Size of buffer
- *C*=Counter of packets in the buffer
- *D*=Delay of packets

4. 1. Simulation Results The MATLAB is used for the simulation purpose and the method used in the simulation is the Monte Carlo simulation in which simulation pattern is based on the random number generation. A random traffic model is used in the simulation process. This is a very simple model but it provides deep inside of the switch performance and effect of variation of parameters on switch. It is assumed in the random traffic model:

- The probability of packet arriving at any of the input is *p*.
- The probability of each packet to go to any of the output is equal and is equal to 1/*N*; here *N* is the total number of output ports in the switch.

The probability that *K* packets arrive for a particular tagged output is given by [9]

$$P[K] = {}^{N}C_{K}\left(\frac{p}{N}\right)^{K}\left(1-\frac{p}{N}\right)^{N-K} \quad (8)$$

It can be observed from the Figure 4 that for a particular value of switch size *N*=16 here, and for fix buffer size let say *m*=4, as load increases delay increase due to more contention between arriving packets. Whereas for lower values of load less than 0.6 we see that the graphs nearly converge because as the incoming traffic is less, there is less contention and data switched fast from input to output port.

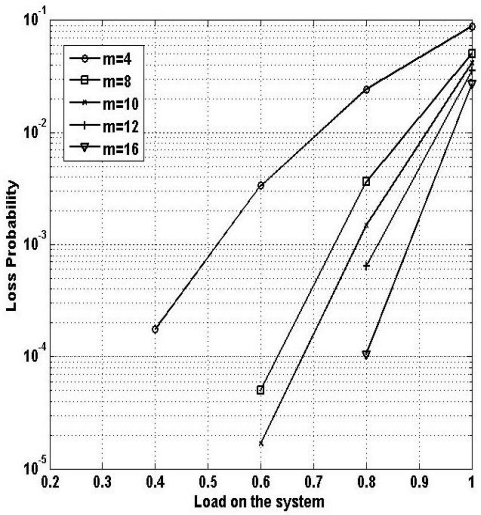

Figure 4. Packet loss probability vs. load (Random Traffic)

As the load increases beyond 0.8 the buffer is more used due to the frequent arrivals of packets and hence it reaches its optimal value. Thus, delays the packets face mainly depend on the traffic arrival rate.

In the first case, we assume that the full buffer capacity can't be utilized due to the physical layer limitations. Considering Table 3, if power level of 2μW is used then to maintain sufficient signal quality, it can correctly receive at the output with BER≤10^{-9}. So, the maximum number of packets stored for a particular output is only 10. In the switch, when ever packet passes through the switch, they are either buffered or they are directed towards its destination port directly. Both type of packets (either buffered or directly transmitted), will have different powers, and due to the signal degradation it may be possible that some of the buffered packets may not be received at the output. So, due to the degrade signal quality the packet may occupy the buffered module of delay 8 or 10. However, the available capacity is of 16 packets. Thus, effective buffer capacity (B_{eff} is of 8 or 10 packets, and other module from 11-16) is not in use. Thus, to achieve a very low packet loss probability it is compulsory that both buffered and directly transmitted packet should have same power. This problem can be solved with the help of SOAs which provide variable gain to both buffered and straight through packets.

The average delay is defined as the average time slot for which packets stays in the buffer before they served towards outputs. The Figure 5 shows a graph between average delays vs. load on the system. Here, the number of inputs and outputs are assumed to be 16 and size of the buffer varies from 4 to 16. As the load on the switch increases the average delay increases. Also, we see that at a particular load as the size of the buffer increases the delay increases. It is also observed from the figures till load of 0.6 due to the lesser arrivals of packets, delay is independent of buffer modules.

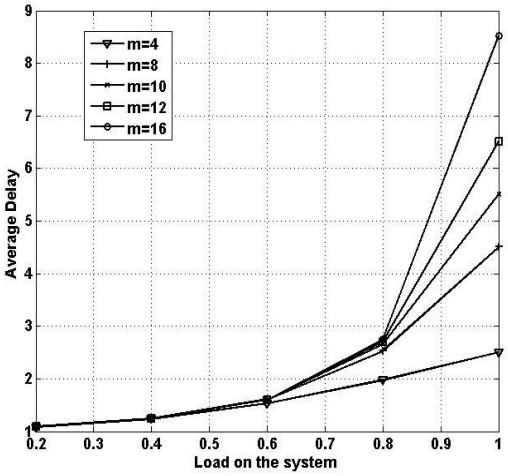

Figure 5. Average Delay vs. Load (Random Traffic)

However, as the load crosses the load of 0.8, there is exponential rise in the delay. This is expected due to the more number of arrivals of packets.

The packet loss probability vs. Load on the system is represented in Figure 6 which we assume a 32×32 node switch, that means 32 inputs and 32 output ports are used in the switch and 32 packets can be buffered in the switch. In the figure, there are total of three curves; two of them are for architecture A1 which are reported in two different papers [22, 23]. For different switch, design and packet loss is presented in the paper [22] and for improving the packet loss rate a load balancing algorithm is presented in the paper [23]. The third curve is used for architecture A2 which is presented in this paper.

The Figure 6 represents that the performance of architecture A1 is much inferior in comparison to architecture A2. At all loads, the difference in packet loss rate is considerable. The packet loss rate, at the load of 0.7 is in order of 10^{-10}, 10^{-5}, and 10^{-3} respectively. Thus, the difference in packet loss rate is very high.

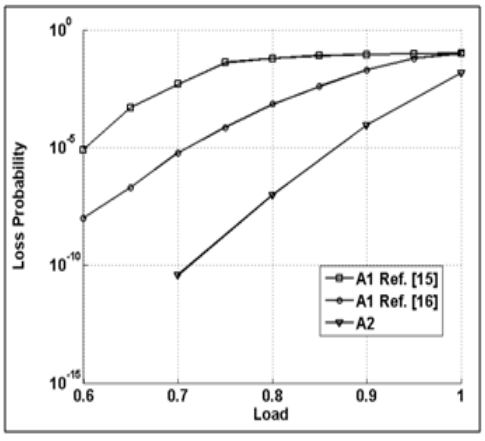

Figure 6. Loss probability vs. load for A1 and A2

5. CONCLUSIONS

This paper discusses the various design issues in optical packet switching system. The analysis of the switch is performed both at physical land network layers. The major concluding remarks of this paper are:

- As the number of buffer modules increases keeping number of inputs fix, the packet loss probability also improves.
- At load values greater than 0.5 to achieve low packet loss probability of order 10^{-4} buffer required for switch size 16 × 16 is at least 8 or above. On decreasing buffer size loss increases and is less than 10^{-3}.
- At near about full load of 0.8 or above, buffer modules required becomes approximately equal to number to inputs. For N=16, if traffic load on switch is suppose 0.8 then required buffer size is at least 16 to achieve low packet loss. Hence, it can be said that the buffer is to fully utilized with $B_{MAX}=N$ to get an optimum switch design at network layer.
- However, to design a switch which is optimum at both physical layer and network layer, the full buffer capacity can't be utilized due to the physical layer limitations. This is called buffer under utilization. This is proved as we saw that though full buffering capacity was of 16 packets but effective buffer space due to the power constraints is B_{eff} equals to 8 or 10.
- Average Delay a packet suffers in the optical node depends on the packet arrival rate.
- To reduce packet drop buffer has to be increased, but this also increases the average delay value.
- We also see that at a particular load as the size of the buffer increases the delay also increases.

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چکیده

این مقاله، طراحی یک سوئیچ نوری بر پایه صف آرایی شبکه موجبر (AWG) را اثبات می کند. در طراحی، هم تجزیه و تحلیل فیزیکی و هم لایه شبکه ای انجام شده است. تجزیه و تحلیل قدرت لایه فیزیکی و سر و صدا برای به دست آوردن نرخ خطای بیت (BER) انجام شده است. دریافته شد که در نرخ بیت بالاتر، BER با تعدادی از ماژول بافر تحت تاثیر قرار نمی گیرد. تجزیه و تحلیل لایه شبکه برای به دست آوردن عملکرد در شرایط نرخ از دست دادن بسته و تاخیر متوسط انجام شده است. تجزیه و تحلیل ارائه شده در مقاله به وضوح نشان می دهد که میزان حداقلی از قدرت مورد نیاز است که برای عملکرد رضایت بخش سوئیچ هم در لایه فیزیکی و هم شبکه ای لازم می باشد.

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