ULTRA-WIDBAND DISTRIBUTED AMPLIFIER UING LOSS COMPENSATION TECHNIQUE ON BOTH INPUT AND OUTPUT CIRCUIT

Mahmoud Mohammad-Taheri

Department of Electrical and computer Engineering, Faculty of Engineering, University of Tehran Tehran, Iran, mtaheri@ut.ac.ir

Mohammed I. Elmasry

Department of Electrical and Computer Engineering, Faculty of Engineering, University of Waterloo Waterloo, Ontario, Canada, N2L 3G1, elmasry@uwaterloo.ca

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Abstract In this paper, we analyze a distributed amplifier based on input/output attenuation compensation. The analysis is carried out for a HEMT transistor; and a constant-k section filter is used to calculate the amplifier's characteristics such as attenuation factor, phase constant and gain. The proposed design approach enables us to examine the tradeoff among the variables, which include the type and the number of devices, and the impedance and cutoff frequency of the lines. Consequently, we arrive at a design which gives the desired frequency response with significant bandwidth enhancement of around 70% with about 10% increase in circuit size. The simulation carried out by Advance Design System (ADS) software. Excellent agreement is shown when the theoretically predicted response of a typical amplifier is compared with the result of the computer-aided analysis (simulation).

Key Words Distributed Amplifier, HEMT, Loss Compensation, Bandwidth Enhancement

چکیده در این مقاله یک تقویت‌کننده گسترده با پهنای باند بسیار زیاد با استفاده از کاهش تلفات اهمی و خازن‌های پارازیتیک در هر دو مدار ورودی و خروجی ترانزیستور HEMT مورد تجزیه و تحلیل قرار می‌گیرد. برای این کار از مدل فیلتر k (k-constant) به جای هر طبقه استفاده شده و بر اساس این مدل پارامترهای تقویت‌کننده نظیر امپدانس مشخصه، فاکتور تضعیف، ثابت فاز و گین محاسبه می‌شوند. این آنالیز به طراح اجازه می‌دهد که مصالحه‌ای بین پارامترهای تقویت‌کننده نظیر نوع ترانزیستور، تعداد طبقات، فرکانس قطع خطوط انتقال بین طبقات و امپدانس مشخصه این خطوط در جهت به دست آوردن یک پاسخ فرکانسی بهینه از نظر گین و پهنای باند صورت گیرد. با روش ارایه شده در این مقاله می‌توان پهنای باند تقویت‌کننده را تا ۷۰٪(با تنها افزایش اندازه حدود ۱۰٪) افزایش داد. در پایان با شبیه‌سازی نشان خواهیم داد که مشخصات تقویت‌کننده طراحی شده با مشخصات خواسته شده مطابقت خوبی دارد.

1. INTRODUCTION

High speed digital communication systems require very wide band amplifiers that are capable of handling pulses with widths in the region of tens of picoseconds. Distributed amplifiers offer a very attractive option for satisfying this requirement, and have been convincingly demonstrated in both monolithic and hybrid solid-state amplifiers [1]-[3]. The principle of distributed or traveling–wave amplification using discrete transistors is a technique whereby the gain-bandwidth product of an amplifier may be increased. In this approach, the input and output capacitances of the transistors are combined with lumped inductors to form artificial transmission lines. This principle is based on neutralizing the bandwidth limiting effects of active devices parasitic capacitances by making them part of the artificial transmission lines that link the active devices. In 1935, W. S. Percival

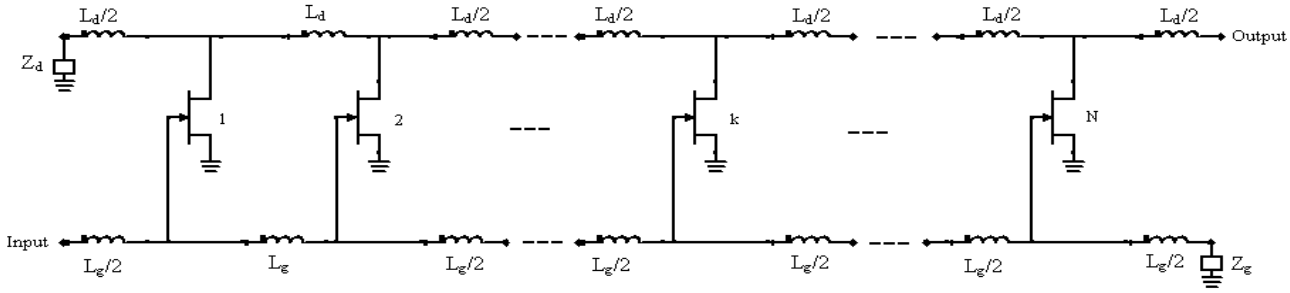

Figure 1. Schematic of FET distributed amplifier.

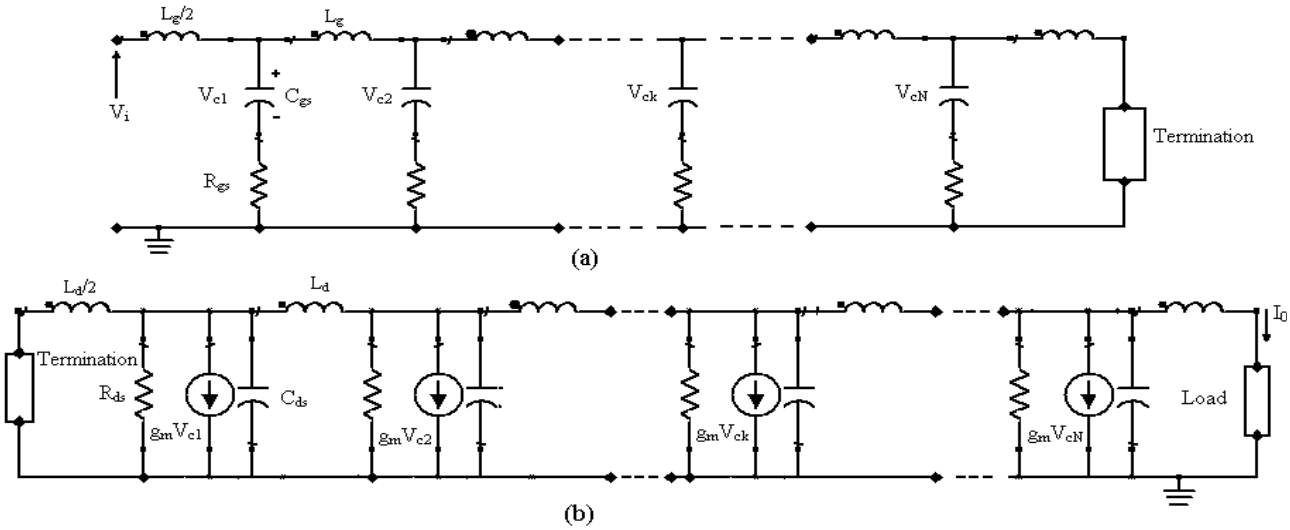

Figure 2. (a) Gate-transmission line and (b) Drain transmission line.

first demonstrated this concept [4]. The lines are coupled by the transconductances of the devices. In a distributed amplifier, the signal is a decaying wave on the input transmission line, and is growing on the output transmission line. At low frequencies, the decay rate is low on input line and the growth rate is high on the output line; at high frequencies, the reverse is true, leading to a lower gain.

The topology of a distributed amplifier is particularly appropriate for Monolithic Microwave Integrated Circuits (MMICs), because its passive circuit predominantly consists of inductors which can be realized in the form of short length of microstrip or coplanar waveguide (CPW) lines. In this paper, we analyze the MESFET distributed amplifier and concentrate on various loss compensation techniques. These techniques are implemented to increase the bandwidth of distributed amplifiers.

2. DISTRIBUTED AMPLIFIER ANALYSIS

A conventional distributed amplifiers (DA) circuit consists of periodically spaced field effect transistors (FETs), which are interconnected by inductors which are realized by electrically short, high impedance microstrip or coplanar waveguide lines as depicted in Figure 1 [5]. A DA design may be qualitatively described as a set of artificial input and output lines coupled by FET transconductances. One important point in the design of a DA is that the line attenuation parameters, α_g and α_d, control the gain and bandwidth. The input (gate)

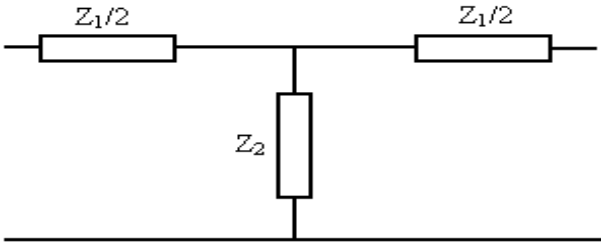

Figure 3. A T-section model of constant k filter.

and output (drain) lines of the DA (see Figure 1), can be considered to be a cascade of constant-k low pass filters shown in Figure 2. This figure also demonstrates equivalent gate and drain transmission lines. In Figure 2, R_{gs} is the effective input resistance between the gate and source terminal, C_{gs} is the gate-to-source capacitance, R_{ds} and C_{ds} are the drain-to-source resistance and capacitance, respectively, and g_m is the transconductance of the device. The lines are assumed to be terminated in their image impedance at both ends. The output current on the drain line can be found by recognizing that each current generator contributes waves of the form - $\frac{1}{2} I_{dk} e^{\pm \gamma_d k}$ in each direction where $I_{dk} = g_m V_{ck}$ and V_{ck} is the voltage across the k^{th} gate-source capacitor, C_{gs} and $\gamma_d = \alpha_d + j\beta_d$ is the propagation function on the drain line (α_d and β_d are the attenuation and phase shift per section on the drain line respectively). Therefore, the current delivered to the load is expressed by

$$I_0 = \frac{1}{2} g_m \, e^{-\frac{\gamma_d}{2}} [\sum_{k=1}^{N} V_{ck} e^{-(N-k)\gamma_d}] \tag{1}$$

where N is the number of transistors in the amplifier. V_{ck} can be expressed in terms of the voltage at the gate terminal of the k^{th} FET as [6]:

$$V_{ck} = \frac{V_i e^{-(2k-1)\gamma_g / 2 - j\tan^{-1}(\omega/\omega_g)}}{[1+(\frac{\omega}{\omega_g})^2]^{\frac{1}{2}}[1-(\frac{\omega}{\omega_c})^2]} \tag{2}$$

where V_i is the voltage at the input terminal of the amplifier, and $\gamma_g = \alpha_g + j\beta_g$ is the propagation function of the gate line (α_g and β_g are the attenuation and phase shift per section on the gate line respectively). In Equation 2, $\omega_g = 1/R_{gs}C_{gs}$ is the gate-circuit corner frequency, and $\omega_c = 2/\sqrt{L_g C_{gs}} = 2/\sqrt{L_d C_{ds}}$ is the cutoff frequency of the lines.

For a constant-k type transmission line, the phase velocity is a well-known function of the cutoff frequency, f_c, of the line. Because the gate and drain must have the same cutoff frequency, the phase velocities are constrained so that they are equal (such that the phase delays on the gate and drain lines are synchronized). Therefore we have $\beta_g = \beta_d = \phi$. From (1) and (2), I_0 can be expressed as:

$$I_0 = \frac{g_m V_i \sinh[\frac{N}{2}(\alpha_d - \alpha_g)] e^{-N(\alpha_d+\alpha_g)/2} e^{-jN\phi - j\tan^{-1}(\omega/\omega_g)}}{2[1+(\frac{\omega}{\omega_g})^2]^{1/2}[1-(\frac{\omega}{\omega_c})^2]\sinh[\frac{1}{2}(\alpha_d - \alpha_g)]} \tag{3}$$

To calculate the power gain of the amplifier, we must calculate the image impedance of the gate and drain line. Figure 3 illustrates the constant-k equivalent of one section of the gate and drain lines. The image impedance is calculated by the following equation for a constant-k transmission line [7]:

$$Z_i = \sqrt{Z_1 Z_2 (1 + \frac{1}{4} Z_1 Y_2)} \tag{4}$$

where

$$Z_1 = jL_g\omega \,,\; Y_2 = 1/(R_{gs} + 1/jC_{gs}\omega) \tag{5-a}$$

for the gate line and

$$Z_1 = jL_d\omega \,,\; Y_2 = 1/R_{ds} + jC_{ds}\omega \tag{5-b}$$

for the drain line. Substituting Z_1 and Y_2 from (5) into (4), we can calculate the image impedance for

the gate and drain lines as follows:

$$Z_{ig} = (L_g / C_{gs})^{1/2}[1-(\omega/\omega_c)^2 + j(\omega/\omega_g)]^{1/2} \quad (6\text{-a})$$

$$\begin{aligned} Z_{id} &= (L_d / C_{ds})^{1/2}[1/\{1+(\omega_d/\omega)^2\} \\ &\quad -(\omega/\omega_c)^2 + j/\{(\omega_d/\omega)+(\omega/\omega_d)\}]^{1/2} \end{aligned} \quad (6\text{-b})$$

The powers delivered to load and to the input of the amplifier are given, respectively, by

$$P_0 = \frac{1}{2}|I_0|^2 \,\mathrm{Re}[Z_{id}] \quad (7\text{-a})$$

$$P_i = \frac{1}{2}|V_i|^2 \,\mathrm{Re}[Y_{ig}] \quad (7\text{-b})$$

In (6-b), $\omega_d = 1/R_{ds}C_{ds}$ is drain-circuit corner frequency. Substituting (3) and (6) into (7), the power gain of the amplifier ($G = \frac{P_0}{P_i}$) is found as follows:

$$G = \frac{g_m^2 \; R_g R_d \sinh^2[\frac{N}{2}(\alpha_d - \alpha_g)]e^{-N(\alpha_d+\alpha_g)}}{4[1+(\frac{\omega}{\omega_g})^2]\;[1-(\frac{\omega}{\omega_c})^2]\;\sinh^2[\frac{1}{2}(\alpha_d-\alpha_g)]} \quad (8)$$

where $R_g = \sqrt{L_g / C_{gs}}$ and $R_d = \sqrt{L_d / C_{ds}}$ are the characteristic resistances of the gate and drain lines respectively.

Considering an equal termination input/output, we calculate the voltage gain of a single amplifier stage from (8) to be

$$A = \frac{g_m (R_g R_d)^{1/2} \sinh[\frac{N}{2}(\alpha_d - \alpha_g)]e^{-N(\alpha_d+\alpha_g)/2}}{2[1+(\frac{\omega}{\omega_g})^2]^{1/2}\;[1-(\frac{\omega}{\omega_c})^2]^{1/2}\sinh\;[\frac{1}{2}(\alpha_d-\alpha_g)]} \quad (9)$$

As can be seen from (8) and (9), the frequency response of the amplifier is a function of the gate and drain lines attenuation factors, α_g and α_d. From (9), it is obvious that by increasing the number of transistors, N, the voltage gain does not increase. There is an optimum number of N in which the gain is maximum; this is obtained by differentiating (9) with respect to N. The optimum number of devices which maximize the gain at a given frequency is

$$N_{opt} = \frac{\ln(\frac{\alpha_d}{\alpha_g})}{\alpha_d - \alpha_g} \quad (10)$$

From (10), it is clear that in the presence of attenuation, the gain of a distributed amplifier cannot be increased indefinitely by adding devices. This property of a distributed amplifier can be easily explained. As the signal travels down the gate line, each transistor receives less energy than the previous one due to the attenuation on the gate line. Similarly, the signal excited in the drain line by a transistor is attenuated by the subsequent line sections between it and the output port. Therefore, additional transistors not only decrease the excitation of the last device, but also increase the overall attenuation on the drain line.

3. CALCULATION OF ATTANUATION ON GATE AND DRAIN LINES

The expressions for the gate and drain line attenuations can be derived from the propagation function, γ, for the constant-k line equivalent of these lines as shown in Figure 3 which is given by [7]:

$$\cosh(\alpha + j\beta) = 1 + \frac{Z_1}{2Z_2} \quad (11)$$

Substituting Z_1 and Z_2 from (5-a) and (5-b) into (11), we can calculate attenuation factor for the gate and drain, respectively. If we assume that the attenuations are small for both the gate and the drain lines, the left hand side of (11) can be expressed as

$$\cosh(\alpha + j\beta) = \cos\beta + j\alpha\sin\beta \quad (12)$$

in which we use $\cosh\alpha \approx 1$ and $\sinh\alpha \approx \alpha$ because α is small. Substituting (5-a) and (5-b) into (11) and equating the real and imaginary parts

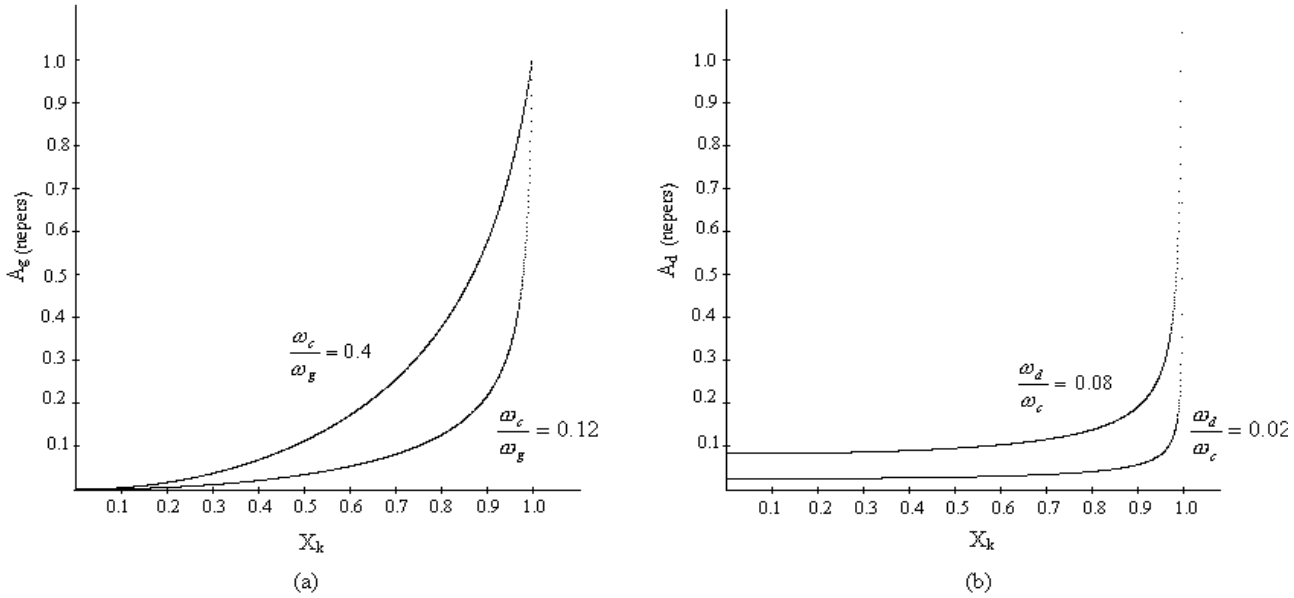

Figure 4. (a) Attenuation on gate line versus normalized frequency and (b) Attenuation on drain line versus normalized frequency.

of (12), we have

$$\alpha_g = \frac{(\omega_c / \omega_g) X_k^2}{\sqrt{1-[1-(\omega_c / \omega_g)^2] X_k^2}} \quad (13\text{-a})$$

$$\beta_g = \cos^{-1} \frac{1-2X_k^2}{1+(\omega / \omega_g)^2} \quad (13\text{-b})$$

$$\alpha_d = \frac{\omega_d / \omega_c}{\sqrt{1-X_k^2}} \quad (14\text{-a})$$

and

$$\beta_d = \cos^{-1}(1-2X_k^2) \quad (14\text{-b})$$

where $X_k = \omega / \omega_c$ is the normalized frequency. To attain a wide band amplifier, the variations of α_g and α_d, with respect to the frequency must be minimum as much as possible. Figure 4(a) and Figure 4(b) depict the variations of these attenuations versus frequency with ω_c / ω_g and ω_d / ω_c as the parameters. These figures demonstrate that the gate-line attenuation is more sensitive to frequency than the drain-line attenuation. Also it can be seen that the attenuation is dominated by the drain-line attenuation at low frequencies and gate-line attenuation at high frequencies. Moreover, (13-a) and (14-a) indicate that the attenuation on the gate and drain lines can be decreased by choosing devices that have high ω_g and low ω_d. Figure 4(a) and Figure 4(b) further show that the variation of the attenuations, with respect to frequency is less when ω_g is high and ω_d is low. It is evidence from (13-b) and (14-b) that with a high ω_g (much greater than amplifier bandwidth), $\beta_g = \beta_d$ as we assumed before. For example, for a typical 300-μm MESFET, f_g=84.2 GHz and B=16.52 GHz, $\max[(\frac{\omega}{\omega_g})^2] = (\frac{16.52}{84.2})^2 < 0.04$.

4. ATTENUATION COMPENSATION AND BANDWIDTH ENHANCEMENT

As we discussed in the previous section, to

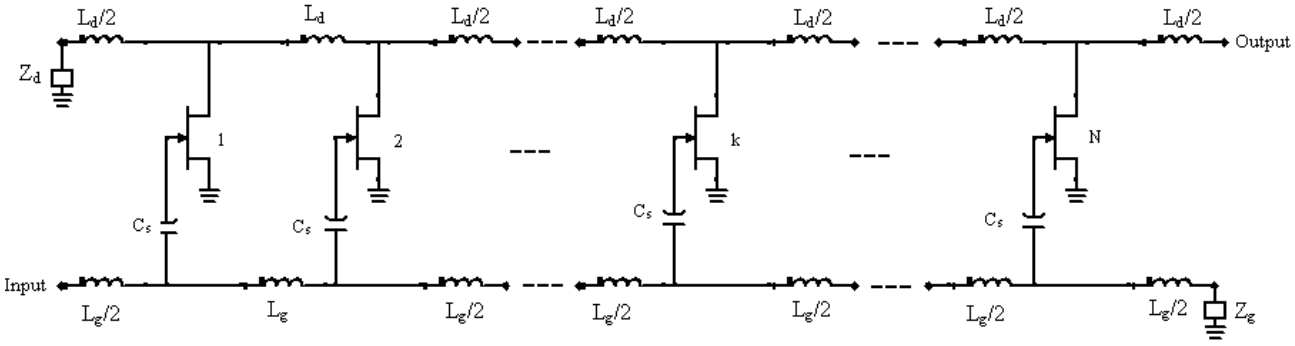

Figure 5. Schematic of a distributed amplifier with series capacitors at FET gate.

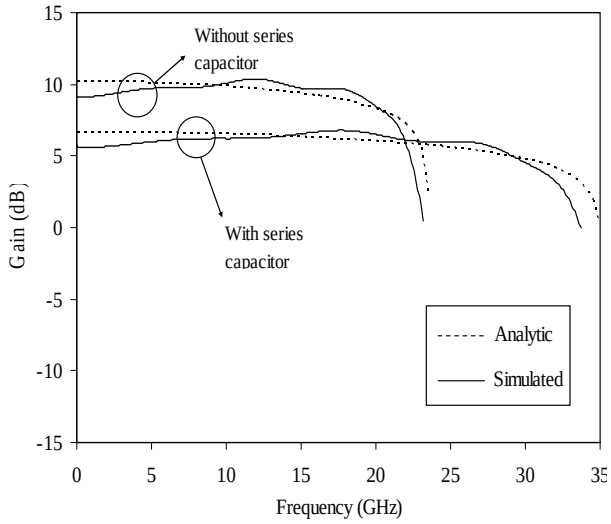

Figure 6. Frequency response of four-stage distributed amplifiers with and without series capacitors at FET gate.

decrease the attenuation we need to increase ω_g and decrease ω_d. To increase ω_g, we must decrease R_{gs} and C_{gs} and to decrease ω_d, we must increase R_{ds} and C_{ds}. Increasing ω_g and decreasing ω_d also increases the bandwidth of the amplifier as shown in Figure 4(a) and Figure 4(b). R_{gs} is reduced by introducing a series negative resistance to the gate and R_{ds} is increased by adding a parallel negative resistance to the drain. In other hands, C_{gs} can be decreased by adding a series capacitor to the gate and C_{ds} c an be increased by adding a shunt capacitor to the drain.

4.1. Decreasing Gate-Line Attenuation by Decreasing C_{gs}

As we mentioned in section 4, to decrease gate-line attenuation a series capacitor must be connected to the gate. If a series capacitor, C_s ($C_s = aC_{gs}$), is connected to the gate as depicted in Figure 5, the effective gate-source capacitance becomes $C'_{gs} = \frac{a}{a+1} C_{gs}$, and the effective gate-line corner frequency becomes $\omega'_g = (1+\frac{1}{a})\omega_g$. Therefore, the gate-line attenuation, α_g, decreases by a factor of approximately $\frac{a}{a+1}$ as shown by (13-a). The FET can now be considered to be a modified device having an effective transconductance of $g'_m = \frac{a}{a+1} g_m$, and an effective capacitance of $C'_{gs} = \frac{a}{a+1} C_{gs}$. The cutoff frequency of the gate and drain lines of a distributed amplifier can be also given by

$$f_c = \frac{1}{\pi R_0 C_{gs}} \tag{15}$$

for which R_0 is the gate or drain characteristic resistance. In the presence of a series capacitor, the

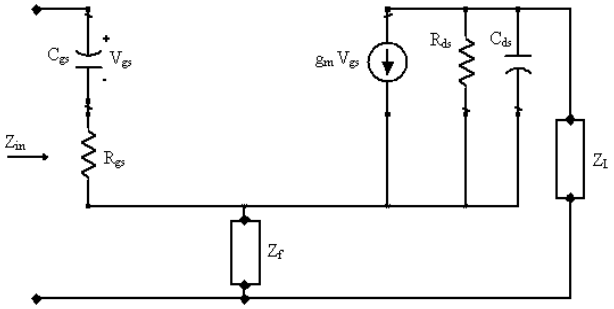

Figure 7. A FET with series feedback element Z_f at the source.

cutoff frequency becomes

$$f_c' = \frac{1}{\pi R_0 C_{gs}'} \tag{16}$$

The bandwidth of the amplifier is proportional to the cutoff frequency of the gate and drain lines. Therefore, if the bandwidth, in the absence of the series capacitor is *B,* and in the presence of the series capacitor, is B', then we attain

$$\frac{B'}{B} = \frac{f_c'}{f_c} = \frac{C_{gs}}{C_{gs}'} = 1 + \frac{1}{a} \tag{17}$$

Therefore, by decreasing *a*, the bandwidth increases. However because the effective transconductance is reduced by a factor of $\frac{a}{a+1}$, the gain will reduce by this factor and the gain bandwidth product (GBP) will be unchanged. The gain can be increased by connecting more FETs, cascading amplifiers, or increasing the gate periphery of the individual FETs as described in [8].

Figure 6, illustrates the frequency response of four-stage distributed amplifier with and without a series capacitor connected to the gate and indicates that the bandwidth is significantly increased by connecting a series capacitor.

We can also see a comparison of the results of the simulation. The analytical results are in good agreement with the simulated results. The gain, however, has decreased as mentioned in this section. The large bandwidth enhancement is due to this fact that, by decreasing C_{gs}, both ω_g and ω_c increase.

4.2. Decreasing Gate-Line Attenuation by Decreasing R_{gs} To decrease the loss in the input line, the gate-source resistance, R_{gs}, can also be reduced as mentioned in section 4. To decrease this resistance, a series feedback needs to be introduced into the FET circuit, which is an impedance element that connects the source to the ground. This is evident in Figure 7, in which the series element Z_f is introduced into the source circuit. The magnitude and phase of Z_f determine the input loss. The input impedance of this configuration is given by:

$$Z_{in} = R_{gs} + \frac{1}{j\omega C_{gs}} + Z_f + \frac{Z_f g_m}{j\omega C_{gs}} \tag{18}$$

The positive real part of Z_{in} represents the input loss. It is obvious that the inductive or resistive component of Z_f contributes to the loss, whereas the capacitive Z_f, yields an input impedance, which has a real part that is less than R_{gs}. In other words, the real part of the sum of the last three terms of (18) is negative when Z_f is capacitive. This condition is easily satisfied when Z_f is a parallel RC combination with a time constant of:

$$RC > C_{gs} / g_m \tag{19}$$

The effective input resistance and capacitance of the transistor can be obtained from the real and imaginary parts of (18) as follows:

$$R_{gs}' = R_{gs} + \frac{R}{1 + (\omega RC)^2}(1 - q) \tag{20-a}$$

and

$$C_{gs}' = [\frac{1}{C_{gs}} + \frac{Rg_m}{(1 + \omega^2 R^2 C^2) C_{gs}} + \frac{R^2 \omega^2 C}{1 + (\omega RC)^2}]^{-1} \tag{20-b}$$

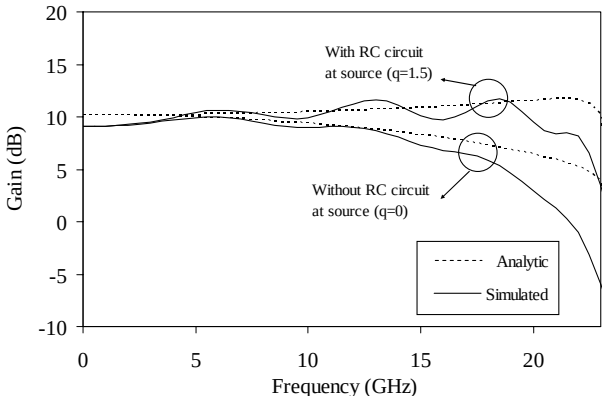

Figure 8. Frequency responses of four-stage distributed amplifiers with and without series feedback element at the FET source.

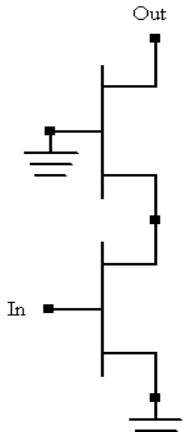

Figure 9. A cascode amplifier configuration.

where $q = RC/(C_{gs}/g_m)$. The inequality in (19) ensures that $q>1$, and according to (20-a), the transistor effective input resistance is less than R_{gs}; the effective R_{gs} of transistor is reduced. Figure 8 shows the frequency response of a typical distributed amplifier for q=0 (uncompensated) and q=1.5 (compensated). We can see that the bandwidth increases for q=1.5. The results of the simulation are also shown for comparison. A good agreement is evident between the analytical and simulated responses.

4.3. Decreasing Drain-Line Attenuation by Increasing R_{ds}

As we have described in section 4, attenuation can also be decreased by decreasing ω_d. This parameter is proportional to the inverse of R_{ds} and C_{ds}. Therefore, to decrease ω_d, we need to increase R_{ds}. Solid-state devices that have an infinite resistance result in no attenuation and no roll-off in the image impedance. The proposed method is to increase the effective resistance by means of a negative resistance. The parallel combination of R_{ds}, and a negative resistance slightly greater than R_{ds} in magnitude will produce a large effective output resistance. The negative resistance is implemented with an ideal negative resistor. The modification of R_{ds} (by shunting a negative resistance) allows for relatively constant image impedance from a very low frequency to the upper cutoff frequency of the amplifier. This provides a superior impedance matching of the line over the entire band. In this regard, the stability consideration is a main issue and a proper design should be carried out to prevent unstability, which has been fully explained in excellent paper by Deibele and Bayer [9].

A widely used circuit for introducing a negative resistance into a drain is a cascode amplifier depicted in Figure 9. This amplifier consists of a combination of common source and common gate FET transistors. The output transmission line is connected to the drain of a common gate transistor and the input line is connected to the gate of a common source transistor. If the gate is terminated with the impedance Z_g, it can be easily shown that the impedance seen from the drain of the common source transistor is [9]

$$Z_d = \frac{R_{ds}}{1 + j\omega\omega_{ds}C_{ds}}[1 + \frac{g_m Z_s}{1 + j\omega\omega_{gs}(R_{gs} + Z_s + Z_g)}] + \frac{Z_s[1 + j\omega\omega_{gs}(R_{gs} + Z_g)]}{1 + j\omega\omega_{gs}(R_{gs} + Z_s + Z_g)} \quad (21)$$

where Z_s is the impedance connected to the source. In fact Z_g and Z_s model the bias and termination loads. Assuming $g_m = |g_m|e^{-j\omega\tau}$ for which τ is the

transient time, it is obvious that the real part of the second term in the bracket is negative if Z_s is highly reactive. At a very low frequency, assuming $Z_s = -jX_s$, the real part of (21) can be simplified as

$$\mathrm{Re}(Z_d) = R_{ds}(1 - g_m X_s \sin \omega\tau) \tag{22}$$

For the case in which Z_s is infinite, (21) can be written as

$$Z_d = \frac{R_{ds}}{1 + j\omega\omega_{ds} C_{ds}} + \frac{1}{j\omega\omega_{gs}} + R_{gs} + Z_g + \frac{g_m R_{ds}}{j\omega\omega_{gs}[1 + j\omega\omega_{ds} R_{ds}]} \tag{23}$$

As can be seen from (23), the only fifth term has negative real value, which is equal to

$$\mathrm{Re}\left[\frac{g_m R_{ds}}{j\omega C_{gs}[1 + j\omega C_{ds} R_{ds}]}\right] = -\frac{g_m R_{ds}}{\omega_d C_{gs}[1 + (\frac{\omega}{\omega_d})^2]} \tag{24}$$

It is interesting to note that the first term of (21) and (23) is the output impedance of a conventional common source FET (Z_s =0). In fact, the real part of the drain impedance has been reduced by the absolute value of the right-hand side of (24). Figure 10 illustrates the frequency responses of a conventional common source, and a cascade distributed amplifiers. As can be seen from this figure, bandwidth has been increased by using a cascade amplifier. The results of simulation are also shown for the comparison. Again the analytical response is in a good agreement with the simulated response. It should be noted that a high transconductance transistors are required to increase the effectiveness of the cascade configuration, which is indicated by (24).

4.4. Attenuation Compensation in Input/ Output Lines for Bandwidth Enhancement

By using a combination of the above techniques we can increases bandwidth considerably and reduce the attenuation. Figure 11 depicts the frequency responses of uncompensated and compensated amplifiers (on both input/output lines). A considerable bandwidth enhancement (around 70%) has been obtained by using attenuation compensation techniques on both the input/output lines. However due to the adding capacitors to the gate of transistor and considering the size of these capacitors, the total size of designed amplifier increases by only 10%. The frequency responses obtained by simulation are also shown in this figure and again a good agreement is evident between analytical and simulated responses.

5. CONCLUSION

In this paper, we have developed an advanced design technique based on attenuation compensation on both the input and output lines of a P-HEMT distributed amplifier. It is shown that a significant bandwidth enhancement of 70% with about 10% increase in circuit size can be obtained, when attenuation compensation circuits are used in both the input and output lines. The compensation allows the use of a higher number of transistors in amplifier configuration, which is a limited factor in a conventional distributed amplifier. It is also shown that, reducing C_{gs} has the most effect in bandwidth enhancement.

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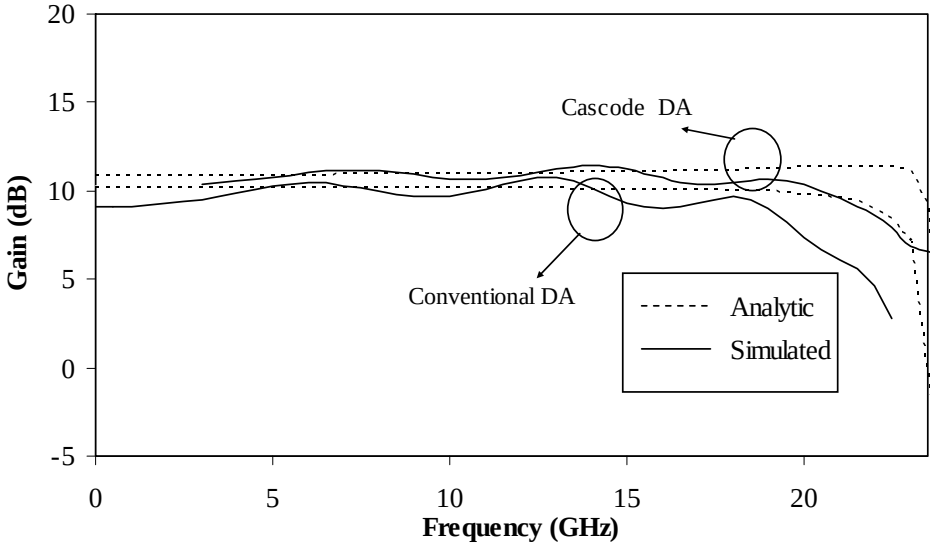

Figure 10. Frequency responses of four-stage conventional and cascode distributed amplifier.

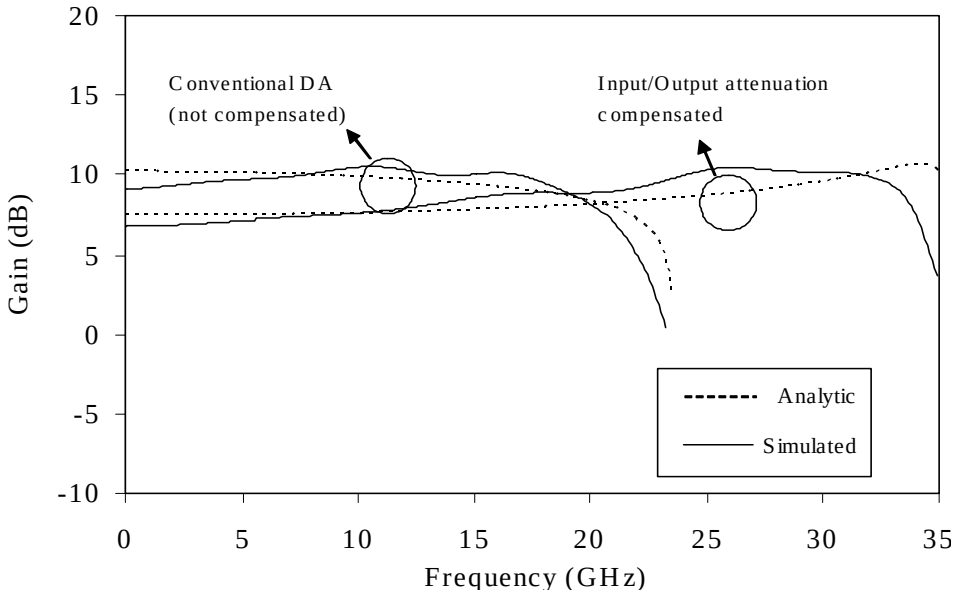

Figure 11. Frequency response curves for conventional and input/output attenuation compensated distributed amplifiers.

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