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Improved Performance Analysis and Design of Dual Metal Gate FinFET for Low Power Digital Applications

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ABSTRACT

A High-K Dielectric Dual Metal Gate FinFET (DMG-FinFET) is proposed in this work to improve the drain current and electrical characteristics of the device. The proposed device employing dielectric materials such as Silicon dioxide, Hafnium oxide and Titanium oxide and investigated in 10 nm technology. The architecture represents a critical advancement in transistor design, addressing challenges posed by traditional high-K gate dielectric materials being HfO_2 and TiO_2. This work employs a comprehensive approach, incorporating simulation techniques to evaluate the performance metrics of DMG FinFET. This investigation encompasses key aspects being transistor characteristics, power consumption, and reliability. This high-k dielectric (HfO_2) Dual material Gate –FinFET device achieving improved performance parameters such as Ion= 32.12 mA, Ioff= 33 µA, Gm(max) = 0.045 S, Gds(max) = 0.024 S and Ron(max) = 32.87 kΩ. Therefore this work is suitable for designing high performance devices with high-k dielectric materials being HfO_2 and TiO_2. The impact of dual metal gate materials on Ion, Ioff, Gm (max), Gds(max) and Ron(max) is calculated and improved 64% compared to conventional device.

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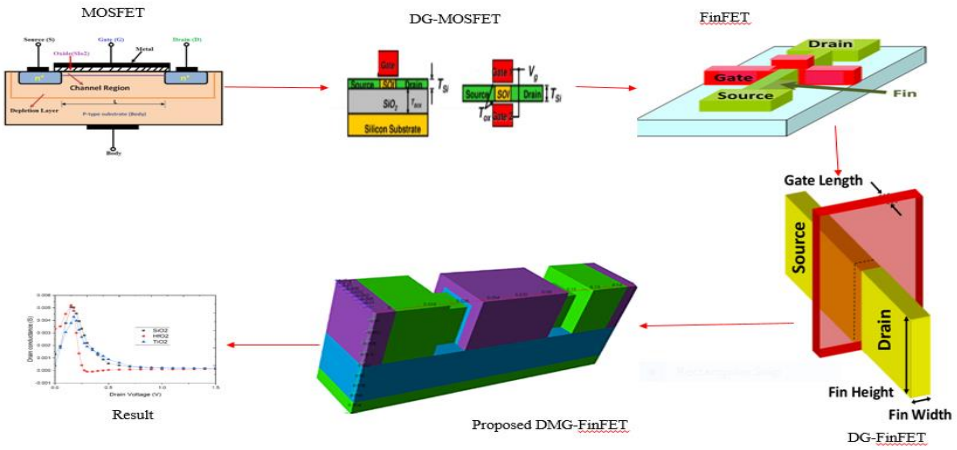
Graphical Abstract



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1. INTRODUCTION

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a crucial component in modern electronics, serving as a fundamental building block for digital and analog circuits. Developed as a successor to the bipolar junction transistor (BJT), MOSFETs play a pivotal role in integrated circuits, enabling the amplification and switching of electrical signals with remarkable efficiency (1). The MOSFET's design leverages the principles of semiconductor physics, offering advantages such as low power consumption, high integration density, and compatibility and comparison with complementary metal oxide-semiconductor (CMOS) technology (2).

The MOSFET has a metal gate that acts as a control electrode. This gate is separated from the semiconductor material by a thin insulating layer, typically made of low-k dielectric materials and high-k dielectric materials such as silicon dioxide (SiO_2), hafnium oxide (HfO2) and Titanium dioxide (TiO_2) (3). The insulating oxide layer isolates the gate from the semiconductor. Its thinness is crucial for facilitating effective control of the transistor. The MOSFET consists of a semiconductor material, often silicon, which forms the channel region where the flow of charge carriers is controlled by the electric field applied by the gate (4). The MOSFET relies on the modulation of the conductivity of the channel region between the source and drain terminals. This modulation is achieved by applying a voltage to the gate terminal, creating an electric field that controls the flow of charge carriers. In an n-type MOSFET, electrons are the majority carriers, and applying a positive voltage to the gate repels electrons, reducing the conductivity of the channel (5). In a p-type MOSFET, holes are the majority carriers, and a negative voltage on the gate serves a similar purpose. MOSFETs are extensively used in digital and analog circuits, serving roles in amplification, signal switching, and as key components in integrated circuits (6). MOSFETs consume minimal power due to their inherent voltage-driven drain current operation and are compatible with CMOS technology, allowing for the integration of large numbers of transistors on a single chip (7). MOSFETs exhibit fast and improved switching characteristics, making them suitable for high-speed digital applications. Therefore, MOSFET is a foundational present trend semiconductor device that has revolutionized the field of electronics. Its versatility, efficiency, and compatibility with integrated circuit technologies have contributed significantly to the miniaturization and performance improvement of electronic devices.

As the quest for more energy-efficient and high-performance electronic devices continues, researchers and engineers are exploring the present novel transistor architectures, and one promising candidate is the Tunnel Field-Effect Transistor (TFET). TFET represents a departure from traditional MOSFETs by leveraging quantum tunneling phenomena to achieve enhanced energy efficiency and reduced power consumption (8, 9). This innovative transistor design holds great potential for applications in low-power integrated circuits and emerging technologies. TFETs operate based on quantum tunneling phenomenon in quantum mechanics where particles can pass through energy barriers that classical physics would consider insurmountable. In the case of TFETs, electrons or holes tunnel through a thin barrier in the transistor's channel region employing with low-k dielectric materials and high-k dielectric materials such as silicon dioxide (SiO_2), hafnium oxide (HfO_2) and titanium dioxide (TiO_2). Similar to MOSFETs, TFETs have source and drain terminals, defining the direction of current flow through the channel. However, the operation of TFETs involves tunneling rather than traditional drift or diffusion of charge carriers (10).

The TFET's energy band diagram plays a crucial role in its operation. With low-k dielectric materials and high-k dielectric materials such as SiO_2, HfO_2 and TiO_2 engineering the bandgap and the tunneling barrier, TFETs can achieve steep subthreshold slopes, a key metric for low-power performance. TFETs have the potential to achieve sub-60 mV/decade subthreshold slopes, surpassing the physical limitations of traditional MOSFETs (11, 12). This characteristic makes them highly attractive for applications where minimizing power consumption is critical. TFETs can operate efficiently at lower supply voltages, contributing to energy savings and enabling the design of circuits with extended battery life in portable devices. TFETs show promise in various applications, including low-power integrated circuits, energy-efficient processors, and devices where extended battery life is crucial (13, 14).

In semiconductor technology, the continual pursuit of smaller transistor sizes and improved performance has led to the development of advanced transistor structures. One such innovation is the Dual Metal Gate FinFET with high-K dielectric materials, a cutting-edge technology implemented in 10nm semiconductor nodes (15). This high-K advanced dielectric materials and transistor architecture addresses the challenges posed by traditional transistor scaling, such as leakage currents and power consumption, thereby enhancing the overall efficiency and performance of integrated circuits (16).

The conventional FinFET technology is widely used in semiconductor manufacturing, particularly in advanced nodes for digital integrated circuits. The process begins with a silicon wafer, which serves as the substrate for the semiconductor device and a thin layer of silicon is deposited on the substrate. A gate dielectric layer is deposited over the fins to control the current.

FinFET (Fin Field-Effect Transistor) is a 3D transistor design that overcomes some limitations of traditional planar transistors. It involves the use of a fin-

like structure for the channel region, enabling better control over the flow of electrical current (17). The dual metal gate refers to the incorporation of two distinct metal layers in the gate structure of the FinFET. This dual-layer design enhances control over the transistor's conductivity and allows for improved performance, reduced leakage currents, and enhanced reliability. The semiconductor industry has witnessed a relentless pursuit of improved miniaturization to enhance performance and energy efficiency (18). As the semiconductor industry progresses towards smaller nodes, the 10nm process emerges as a promising device. This study focuses on the qualitative performance analysis of dual metal gate (DMG) FinFET (DMG-FinFET) in the 10 nm technology node (19).

Power efficiency is a critical concern in modern semiconductor design. The analysis delves into the power consumption patterns of DMG FinFETs under various operating conditions being dynamic power consumption during switching events and static power dissipation in idle states (20). This work investigates the robustness of DMG FinFETs in the face of process variations and environmental factors, providing insights into their long-term performance related to low-K dielectric materials and high-K dielectric materials such as SiO_2, HfO_2 and TiO_2 (21).

Traditional transistors use silicon dioxide (SiO_2) as the gate dielectric. However, as transistors shrink, the insulating properties of silicon dioxide diminish. High-K dielectric materials, characterized by a higher dielectric constant (K), are employed to counteract this effect. Common high-K materials include hafnium oxide (HfO_2) -based compounds, which offer better insulation and allow for further downscaling of transistor dimensions. The high-K dielectric materials help minimize leakage currents, enhancing the energy efficiency of the transistors. The dual metal gate design provides better control over the transistor's conductance, resulting in improved speed and performance. The 10nm technology allows for the fabrication of smaller, more densely packed transistors, contributing to increased device integration and overall performance. The DMG FinFET with high-K dielectric materials in 10nm technology finds applications in a wide range of electronic devices, including smartphones, tablets, high-performance computing systems, and other advanced electronic devices demanding higher processing power and energy efficiency (22).

2. DEVICE STRUCTURE AND MODELLING

The fabrication process for FinFETs is more complex compared to traditional planar transistors, requiring additional manufacturing materials and increased process control. The complexity of the FinFET fabrication process, along with the need for advanced materials and equipment, can lead to higher manufacturing costs. Variability in the height of the fin structures can occur during the fabrication process, leading to performance variations among transistors. This variability can affect the overall yield and reliability of the semiconductor device.

The design of a DMG FinFET with high-K dielectric material such as silicon dioxide (SiO_2), hafnium oxide (HfO_2) and titanium dioxide (TiO_2) involves several key considerations to optimize device performance, reduce power consumption, and ensure manufacturability. In this proposed HfO_2 DMG-FinFET, employing a suitable semiconductor material for the fin structure as silicon and gate dielectric materials as HfO_2 and TiO_2 as shown in Figure 1. The fin provides the channel through which the current flows. The high-K dielectric material, such as hafnium oxide (HfO_2), to replace traditional silicon dioxide as the gate dielectric. High-K materials enable effective gate control and minimize leakage currents. The proposed high-K FinFET architecture to enhance control over the channel. The fin structure allows for better electrostatic control of the channel, reducing leakage current and improving overall transistor performance. Design a gate stack in the proposed device that includes the high-K dielectric layer and the metal gates. Optimize the thickness and composition of each layer to achieve the desired electrical characteristics, such as threshold voltage and subthreshold slope (23).

The high-K dielectric material, HfO_2 device fin for optimal carrier mobility and electrostatic control. Consider the fin width, height, and doping concentration to achieve the desired device characteristics. In this proposed device spacer engineering dielectric material being TiO_2 helps in achieving better control over the transistor characteristics and mitigating issues related to process variations. The integration of the DMG FinFET into the semiconductor fabrication process must be seamless to enable large-scale production and 10nm, to leverage the advantages of this high-K dielectric materials being HfO_2 and TiO_2 manufacturing processes (24).

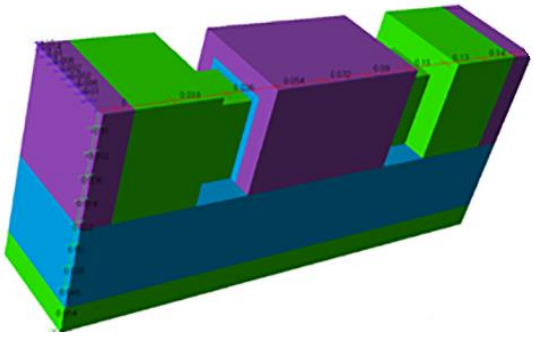

Figure 1. Proposed DMG- FinFET

Utilized the simulation and modeling TCAD tool to predict and optimize the device characteristics before actual fabrication. This aids in fine-tuning the design parameters for optimal performance. Therefore, the proposed device design of DMG-FinFET with high-K dielectric materials, engineers can create transistors that offer improved qualitative performance, reduced power consumption, and enhanced reliability for advanced semiconductor technologies (25, 26). High-K dielectric materials and the FinFET architecture help achieve lower subthreshold slopes, reducing power consumption in subthreshold slop operation (27). This is particularly advantageous for applications requiring energy-efficient operation in low-power states. The use of high-K dielectric materials contributes to improved temperature stability. This is vital for maintaining consistent device performance across a range of operating conditions, ensuring reliability in various environments (28).

Table 1 shows the proposed device utilized parameters for the simulation in 10nm technology. The improved performance parameters of proposed device compared with existing devices are shown in Table 2.

3. PROPOSED DEVICE ALGORITHM

The algorithmic proposed FinFET design determining the materials for the dual gate structure. This could involve optimizing the properties of each SiO_2 and HfO_2 material to achieve higher drain current and lower leakage current performance characteristics. Developing algorithms for the precise placement and control of the dual materials within the gate structure. This may involve considerations for thickness, composition, and other material properties. Implementing algorithms to optimize the manufacturing process, including deposition, etching, and other steps involved in creating the dual material gate FinFET. The development of algorithms to model the electrical characteristics and performance of the dual material gate FinFET. This could include simulations and analyses to predict behavior under various dielectric materials. The algorithms may be developed to seamlessly incorporate the dual material gate FinFET into existing fabrication processes.

The novelty in semiconductor technology often involves improvements in performance, power efficiency and transistor design. In DMG FinFET is a recent development with gate length of 22 nanometer and thickness of Fin is 2nm. The unique features of this device is improved drain current, reduced leakage current and lower sub threshold swing about 64 percent. Therefore, this device is suitable for low power applications.

TABLE 1. Used parameters of the proposed device

Device Parameter	Value
Length of device(W_L)	60 nm
Gate Length(L_G)	10 nm
Source Length(L_S)	30 nm
Drain Length(L_D)	30 nm
Channel Length(L_C)	10 nm
Source Doping(N_D)	10^{18} cm^{-3}
Drain Doping (N_D)	10^{18} cm^{-3}
Channel Doping	10^{20} cm^{-3}
Gate Work Function	4.3eV
Low-k material	SiO_2
High-k material	HfO_2
Fin width	10nm
Fin height	14nm

TABLE 2. Used Modelling for the proposed structure

Model	Description
conmob	Specifies the concentration mobility
fldmob	Calculation of the field dependent mobility
evsatmod=1	implements the carrier temperature mobility
hcte.el	to enable energy balance for electrons
taurel.el	specifies the relaxation time in the
taumob.el	specifies the relaxation time for electrons

4. RESULTS AND DISCUSSION

4. 1. Drain Current Vs Drain Voltage Characteristics Analyzing the characteristics of the drain current (Id) as a function of the drain-to-source voltag (Vds) for a DMG FinFET with high-K dielectric materials being hafnium oxide (HfO_2)and titanium dioxide (TiO_2) involves at low Vds values, below the threshold voltage (Vth), the proposed device is in the subthreshold region. In this region, the drain current is exponentially dependent on Vds. The subthreshold slope is a crucial parameter, and the use of high-K dielectric materials (HfO_2) helps in achieving lower subthreshold slopes, contributing to lower power consumption in subthreshold operation as shown in Figure 2. The threshold voltage is the gate voltage at which the Id begins to conduct. In the $Id\ Vs\ Vds$ plot, this is the point where the curve starts to rise. DMG design can impact the threshold voltage, allowing for better tuning and control. As Vds increases beyond Vth, the transistor enters the saturation region. In this region, the drain current becomes relatively independent of Vds (29, 30).

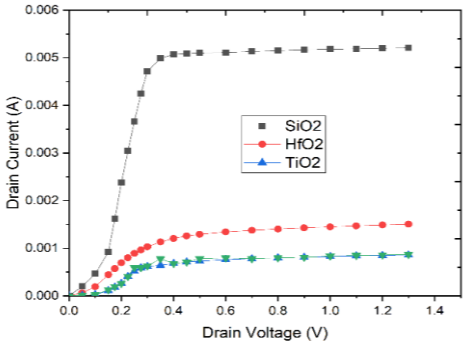

Figure 2. Id Vs Vds characteristics of Proposed device with HfO_2 and TiO_2 high-K dielectric mater

4. 2. Drain Current Vs Gate Voltage Characteristics

The drain current (Id) as a function of gate-to-source voltage (Vgs) measured in volts (V) for DMG FinFET with high-K dielectric materials provides valuable insights into the transistor's behavior. The threshold voltage (Vth) is the gate voltage at which the transistor just starts to conduct. In the Id vs Vgs plot, where the curve begins to rise. High-K dielectric materials such as hafnium oxde (HfO_2) and titanium dioxide (TiO_2) and the dual metal gate design influence Vth, allowing for better control and optimization. At lower Vgs (V) values (below Vth), the transistor is in the subthreshold region. The drain current in this region is exponentially dependent on Vgs. High-K dielectric materials (HfO_2 and TiO_2) help in achieving lower subthreshold slopes, contributing to lower power consumption in subthreshold operation. As Vgs increases beyond Vth, the transistor enters the saturation region. In this region, the drain current becomes relatively independent of further increases in Vgs (V). The dual high-K metal gate design contributes to improved electrostatic control, reducing the impact of gate voltage on the drain current as shown in Figure 3.

4. 3. Drain Conductance Characteristics

The drain conductance is an important parameter in the operation of a proposed DMG-FinFET, employing with high-K gate dielectric materials being HfO_2 and TiO_2. It is a measure of how easily current can flow from the source to the drain terminal of the device. The drain conductance is influenced by high-K dielectric materials as HfO_2 and TiO_2. The drain conductance of a DMG FinFET would be influenced by the specific characteristics of the dual metal gate structure. The choice of high-K dielectric materials and spacer materials, and the overall design of the transistor impact how efficiently current can be conducted from the source to the drain as shown in Figure 4.

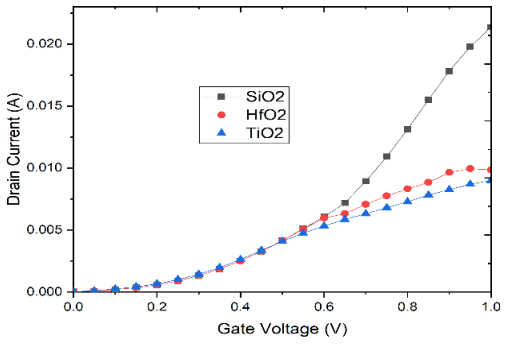

Figure 3. Id Vs Vgs characteristics of Proposed device with HfO_2 and TiO_2 high-K dielectric materials

4. 4. Transconductance Characteristics

The transconductance (gm) of a DMG FinFET with high-K dielectric materials high-K gate dielectric materials being HfO_2 and TiO_2 is a crucial parameter that indicates how effectively the transistor amplifies small input signals. The transconductance of this device is mathematically expressed as the derivative of the drain current (Id) with respect to the gate-source voltage (Vgs) and it is highly dependent on the gate-source voltage. As Vgs increases, the transistor enters the saturation region, where the slope of the Id vs Vgs curve determines the transconductance. In the saturation region of the transistor operation, the slope of the Id vs Vgs curve represents the transconductance. A steeper improved slope corresponds to a higher transconductance and indicates better amplification capability as shown in Figure 5.

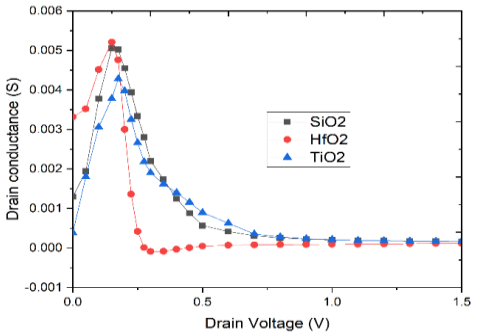

Figure 4. Gd Vs Vds characteristics of Proposed device with HfO_2 and TiO_2 high-K dielectric materials

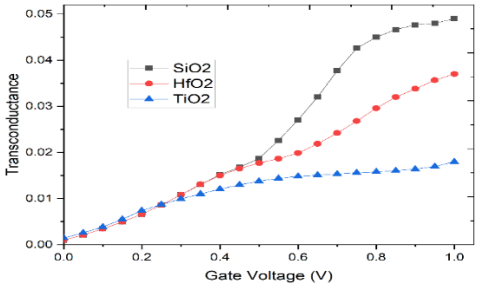

Figure 5. 5 Gm Vs Vgs characteristics of the proposed device with HfO_2 and TiO_2 high-K dielectric materials

The resistance characteristics of a DMG FinFET with high-K dielectric materials are important for understanding the device's behavior in various operating conditions. The channel resistance is a crucial component of the total resistance in a transistor as shown in Figure 6. It is influenced by the properties of the semiconductor material forming the channel and the dimensions of the fin structure. In a FinFET, the 3D fin structure provides better electrostatic control, reducing channel resistance compared to traditional planar transistors. The overlap between the gate and source regions can contribute to resistance. Design considerations, such as optimizing the gate-source overlap and using appropriate materials can impact this resistance as shown in Figure 6. The series resistance of the source and drain regions, including the contact resistances, can significantly affect the overall transistor resistance. Techniques such as silicidation are often employed to reduce source and drain contact resistances.

The reduction of sub threshold slope increases the off-current and power dissipation in the device. These characteristics are essentials for low power portable devices. The amount of gate voltage needed for variation of drain current defined as sub threshold slope given in Equation 1:

$$Subthreshold\ slope\ (SS) = \frac{\partial V_{gs}}{\partial(\log(I_{ds}))} \quad (1)$$

Silicon dioxide (SiO_2) is a key material in semiconductor manufacturing, particularly in the fabrication of integrated circuits. SiO_2 has a high dielectric constant, making it an excellent insulator. This property is crucial for the gate dielectric in metal-oxide-semiconductor (MOS) transistors, where SiO_2 has historically been used and the thickness of SiO_2 is 2nm in proposed in this simulations

4. 5. Main Achievement of the Prposed Device

The DMG-FinFET device contributes to improved electrostatic control, reducing the impact of drain voltage on the drain current. The higher Vds values, the transistor enter a linear region where the drain current increases linearly with Vds. This region is generally not desirable for digital applications but may relevant in certain analog circuit configurations also based on higher drain current, lower leakage current and lower sub threshold swing. The block diagram of proposed device as shown in Figure 7.

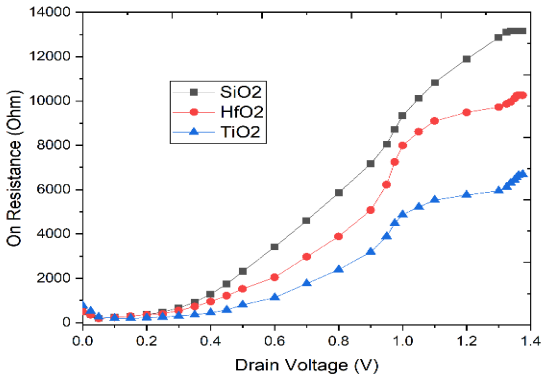

Figure 6. Ron characteristics of Proposed device with HfO_2 and TiO_2 high-K dielectric materials

TABLE 3. Performance parameters comparison with various devices based on literatures work

Parameters	C FinFET	SG FinFET	DG FinFET	HD-DMG FinFET	Proposed Device
Ion (A/μm)	4.13	5.84	5.9	5.93	8.2
Ioff (A/μm)	8.20	8.90	6.22	6.20	2.27
Ion/Ioff	2.29	2.9	3.1	3.81	3.841
Gm (S/mm)	2.31	2.34	2.6	2.61	3.81
Gd (S/mm)	2.1	1.19	1.84	2.8	2.01
Ron (Ωmm)	3.1	2.6	2.14	2.17	3.15

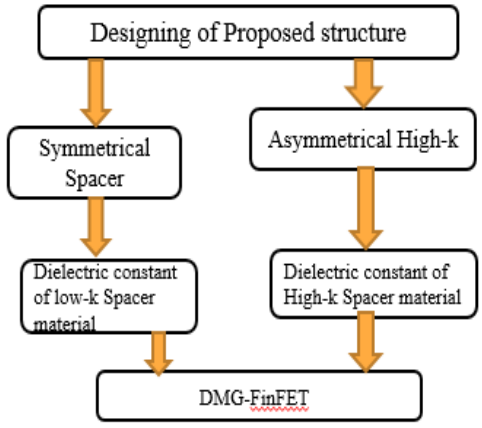

Figure 7. Block diagram of Proposed device

5. CONCLUSION

The integration of Dual Metal Gate FinFET with high-K Dielectric Materials in 10nm technology represents a significant advancement in semiconductor technology, offering a range of benefits for modern electronic devices. The proposed device employing high-K dielectric materials such as hafnium oxide (HfO_2) and titanium oxide (TiO_2) and investigated in 10 nm technology. The dual metal gate design enhances electrostatic control over the channel, reducing leakage currents and improving overall device performance. The incorporation of high-K dielectric materials in the gate stack replaces traditional HfO_2 and TiO_2. The proposed

high-K dielectric materials DMG-FinFET has improved performance over silicon dioxide (SiO_2) gate stack and notable enhancement in device performance and subthreshold slope. The advantages of the proposed structure have the improvement performance compared to existed devices such as drain current and reduced leakage currentin and switching ratio about ~ 12 times is reported. The most recent innovation in this proposed structure lies in the Fin thickness, which is now 2nm and enables precise control of the current across the entire device. The limitations of this proposed structure is SS, which can be reduced in submicron node. The future scope in this proposed device can introduce advanced structural modifications in the optimized FinFET to enhance device further features for very lower applications.

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Persian Abstract

چکیده

یک FinFET دو دروازه فلزی دی الکتریک بالا (DMG-FinFET) در این کار برای بهبود جریان تخلیه و ویژگی های الکتریکی دستگاه پیشنهاد شده است .دستگاه پیشنهادی با استفاده از مواد دی الکتریک مانند دی اکسید سیلیکون، اکسید هافنیوم و اکسید تیتانیوم و در فناوری 10 نانومتر بررسی شده است .این معماری نشان دهنده یک پیشرفت حیاتی در طراحی ترانزیستور است که به چالش های ناشی از مواد دی الکتریک دروازه سنتی با پتاسیم بالا (HfO_2 و TiO_2) رسیدگی می کند.این کار از یک رویکرد جامع استفاده می کند، که هر دو تکنیک شبیه سازی را برای ارزیابی معیارهای عملکرد DMG FinFET ترکیب می کند .این بررسی جنبه های کلیدی مانند ویژگی های ترانزیستور، مصرف برق و قابلیت اطمینان را در بر می گیرد .این دستگاه دی الکتریک با کیفیت بالا (HfO_2) دو ماده گیت FinFET - که به پارامترهای عملکردی بهبود یافته مانند Ion = 32.12 mA، Ioff = 33 µA، Gm (max) = 0.045 S ، Gds(max) = 0.024 S و Ron حداکثر (دست می یابد 32.87 = .کیلو اهم.بنابراین این کار برای طراحی دستگاه های با کارایی بالا با مواد دی الکتریک با k بالا که HfO_2 و TiO_2 هستند مناسب است .تاثیر مواد دروازه فلزی دوگانه بر روی یون،Ioff، Gm (max)، Gds (max)و Ron (max) محاسبه شده و 64 درصد نسبت به دستگاه معمولی بهبود یافته است.