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Investigation and Analysis of Dual Metal Gate Overlap on Drain Side Tunneling Field Effect Transistor with Spacer in 10nm Node

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This paper investigates the electrical behavior and performance of a Dual Metal Gate Overlap on Drain Side Tunnel Field Effect Transistor with Spacer (DMG-ODS-TFET) in 10 nanometer technology. In this design, the utilization of two different metals to create the gate effectively maintains electrostatics and minimizes gate leakage current. This structure is formed by silicon dioxide and hafnium oxide as dielectric materials. The drain current characteristics such as subthreshold swing, on-state current, off-state leakage current, and transconductance are calculated for the proposed device using the available two-dimensional numerical device simulator silvaco tool. The characteristics of the proposed device vary with changes in channel length, doping concentrations of the drain and source, and the thickness of the oxide layer. This structure shows a lower off current, and better on-to-off current ratio with improved drain current. Consequently, the proposed design effectively balances gate control and leakage current, resulting in superior to conventional and dual metal gate devices. Based on improved performance parameters, this proposed structure is suitable for high-frequency applications.

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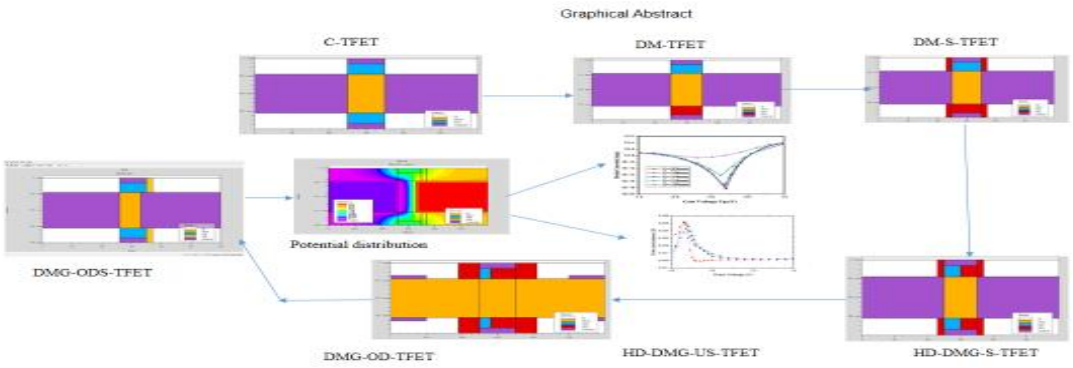
Graphical Abstract



NOMENCLATURE

tox	Oxide thickness	SiO_2	Silicon dioxide
V_{ds}	Drain to source voltage	HfO_2	Hafnium oxide
I_d	Drain Current	*Vgs*	Gate to source voltage
Ion	On state current	*Ioff*	Off state current

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1.INTRODUCTION

The Metal Oxide-Semiconductor Field-Effect Transistor (MOSFET), is a fundamental electronic device used in a wide range of applications, from digital and analog circuits to power electronics. It serves and gives the crucial building block in modern electronic systems, allowing for the control and amplification of electrical signals. MOSFETs are the basic foundation of modern digital integrated circuits (ICs) such as microprocessors and memory chips (1). They are used in various analog applications, including amplifiers, voltage regulators, and analog switches. MOSFETs are employed in high-power applications like motor control, voltage inverters, and switching power supplies. RF MOSFETs are used in wireless communication devices and RF amplifiers. However, due to limited voltage handling capabilities compared to other devices,Tunnel Field Effect Transistor (TFET) have come up in to the semiconductor industry (2). For over five decades, the semiconductor industry has relied on the miniaturization of circuits through the downsizing the length of MOSFET as its primary device (3). However, conventional MOSFETs have limitations, such as a sub-threshold slope limited to 70 mV/decade and strict power constraints after scaling down the devices. Consequently, extensive research has sought alternatives for nano integrated circuits, leading to the adoption of highly energy-efficient TFETs for future applications. TFETs exhibit a sub-threshold slope of less than 70 mV/decade, making them ideal for commercial low-power uses (4).

As the semiconductor industry continues to advance towards smaller nodes and, the development of modern novel transistor designs becomes imperative to maintain performance gains while mitigating power consumption. Therefore, TFETs have garnered significant attention due to their potential to provide steep subthreshold slopes, reduced leakage current, and improved energy efficiency compared to conventional MOSFETs. In this work, the device modelling and the impact of dual metal gate overlap on the drain side of Tunnel Field Effect Transistor (DMG-ODS-TFET) with spacer technology is implemented in 10nm node (5). Both MOSFETs and TFETs are important semiconductor devices used in electronic circuits. While MOSFETs are widely established and versatile, TFETs offer unique characteristics that make them promising devices for specific applications, particularly in low-power and high-frequency domains (6). The choice between these two transistors depends on the specific requirements of the electronic system being designed. The TFET is an advanced semiconductor device that operates based on the principle of quantum mechanical tunneling. It offers unique properties and advantages, making it a promising device in the field of electronics. Researchers continue to explore and develop TFETs to harness their full potential in future electronic systems (7).

The TFETs are emerging as the most promising devices for low-power applications, offering several advantages over MOSFETs. However, a significant limitation of TFETs is their low ON current. Therefore, researchers are actively working on enhancing the ION current in TFETs. One approach involves using high-k dielectric materials to improve mobility and ION current (8). The higher permittivity of these dielectric materials reduces gate dielectric leakage, and metal gates effectively control electrons within the high-k dielectric (9). This addition of high-permittivity dielectric materials enhances carrier mobility in the channel region and increases the ON current of TFETs. In TFETs, the implementation of multiple gate structures provides better control over the channel potential and increases the effective tunneling area, resulting in improved ON current (10). The primary tunneling area in TFETs is at the source-channel junction, and employing multiple gate structures effectively enlarges this tunneling area. Combining multi-material and double-gate TFET devices results in a high ON current. Additionally, increasing the source doping concentration enhances the ON current. To further suppress ambipolar effects and increase the ON current, lower band gap materials are employed. Hetero-junction devices are also used to achieve a lower effective band gap at the source-channel junction (11).

In the evolving field of the semiconductor industry, the rigorou`s pursuit of miniaturization and improved performance has led to the development of advanced transistor structures (12). Among these innovations, the DMG-ODS-TFET has gained prominence in the 10nm technology node. This device explores into the investigation and analysis of a crucial aspect of the proposed device. The rigorous demand for faster and more energy-efficient electronic devices has spurred continuous innovation in semiconductor manufacturing. As silicon technology advances into the 10nm node and beyond, transistor design has become increasingly complex. One notable development in this pursuit of performance optimization is the spacer technology (13).

The advanced DMG-OD-TFET addresses the limitations of traditional TFET designs and enhances performance device parameters in submicron technology (14). This innovative design comprises two components such as a dual metal gate (DMG) and spacer material on the drain side. The hetero dielectric gate stack employs two distinct dielectric materials high-k dielectric material, specifically hafnium oxide (HfO_2), and low-k dielectric material, such as silicon dioxide (SiO_2). By incorporating these dielectric materials into the design, it can optimize the electric field distribution, resulting in improved electrostatic control (15). This enhanced and

improvement will control effectively mitigates ambipolar conduction and significant challenge in TFETs, and enables efficient modulation of advanced device's on/off characteristics. Additionally, the integration of advanced gate overlap on the drain side into the TFET structure with HfO_2. This overlap physically separates the source and channel regions, thereby reducing direct source-to-drain tunneling current, a major contributor to off-state leakage in TFETs. Through the minimization of this leakage current, the underlap spacer enhances the on/off current ratio and overall device performance. However, a comprehensive analysis is essential to understand the impact of these design modifications on various metric devices.

The TFET offers several advantages, including a sub-60 mV/dec subthreshold swing (SS) at room temperature and reduced leakage current. This makes it a promising alternative to traditional MOSFETs for low-power applications. Various techniques have been explored to enhance TFET performance, such as employing graded Silicon and Germanium heterojunction TFETs through bandgap engineering and using dual spacer dielectrics SiO_2 and HfO_2. Additionally, reducing leakage current and subthreshold swing has been achieved by employing a very lightly doped drain material (with ND $\approx 2 \times 10^{18}$ cm−3) with a low density of states, such as Indium Gallium Arsenide. In this design, the length of the lightly doped drain should be limited to around 10 nm. Recent research has demonstrated that TFET performance can be further improved by introducing a non-uniform body thickness (16). In this paper, the two-dimensional cross sectional view and simulations of DMG-OD-TFET with low leakage current and low ON-to-OFF ratio is presented and introduced a new phenomenon called gate overlap on the drain side and demonstrate the presence of off-state current as the channel length is reduced to 10nm.

The DMG-OD-TFET is a promising device for advanced integrated circuits due to its ability to mitigate short-channel effects and improve device performance (17). Spacer technology, which involves the use of dielectric materials around the gate electrode, further enhances transistor performance by reducing leakage currents and improving electrostatic control. The overlap region, where the gate material extends beyond the gate dielectric, plays a pivotal role in device performance (18). It shows directly impacts device characteristics such as threshold voltage, subthreshold swing, and drain-induced barrier lowering (DIBL) (19).

The DMG-ODS-TFET in 10nm Node refers to an advanced semiconductor technology that plays a crucial role in enhancing the performance and energy efficiency of new transistors in the 10-nanometer semiconductor manufacturing process. This technology leverages a DMG design and spacer integration to address drain-induced barrier lowering (DIBL) and improve the overall proposed transistor characteristics in the 10nm node. The 10nm semiconductor manufacturing process in this proposed device signifies a high level of miniaturization and a substantial increase in transistor density compared to previous nodes. This design is crucial for optimizing transistor performance and mitigating various electrical characteristics, drain current, analog characteristics, and RF characteristics. The gate structure extends slightly beyond the drain region of the transistor. This extension is strategically engineered to address issues like DIBL, where the control of the proposed TFET behavior is affected by the voltage at the drain terminal. The proposed DMG-ODS-TFET relies on quantum tunneling for its operation, offering potential advantages in terms of reduced power consumption and improved drain current characteristics compared to conventional TFETs. Spacer materials SiO_2 and HfO_2 are the insulating materials around the gate structure to fine-tune the transistor characteristics and mitigate unwanted electrical effects.

2. DEVICE STRUCTURE AND SIMULATION PARAMETERS

The DMG-ODS-TFET leverages quantum tunneling for electron transport, making it a promising device for low-power applications. In the context of this proposed structure, it has two different gate materials, often used to control different aspects of device performance (20). The proposed device typically consists of a source, a drain, a channel, and a dual gate. The gate is usually separated from the channel by a thin insulating layer, and the gate materials can vary (21). A spacer material was added to this structure to enhance the device characteristics. The 10-nanometer node allows for more transistors per unit area and can offer improved performance and power efficiency. The overlap can impact the device's characteristics, such as threshold voltage and subthreshold swing, which are crucial for TFET performance (22). In this device, electrons tunnel through a thin insulating barrier between the source and the channel, which is different from traditional transistors like MOSFETs, where electrons move through a conductive channel as shown in Figure 1.

The mesh and two-dimensional cross-sectional view of the proposed device and its electric field distribution and potential distributions as shown in Figures 2, 3 and 4.

The TFET technology with other innovations, such as three-dimensional integration and advanced packaging techniques, could lead to enhanced overall system performance. Controlling the doping profiles in the TFET structure, especially in the drain region, can impact the tunneling process. Optimizing the doping concentration and distribution can contribute to better device characteristics.

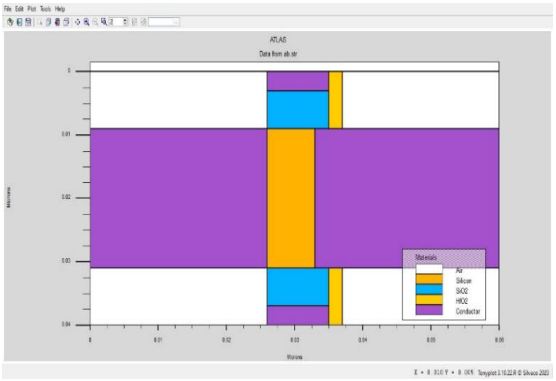

Figure 1. 2 D cross-sectional view of proposed Dual Material Gate Overlap on Drain Side TFET with spacer

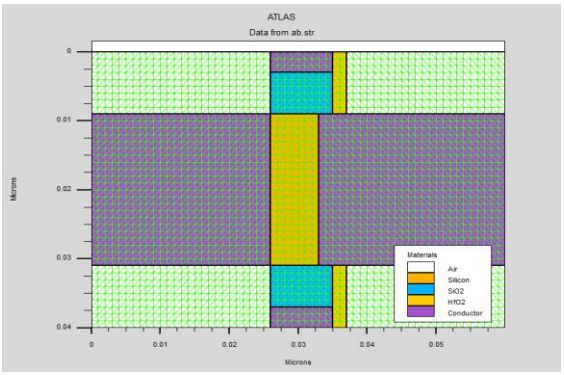

Figure 2. Mesh View of proposed device

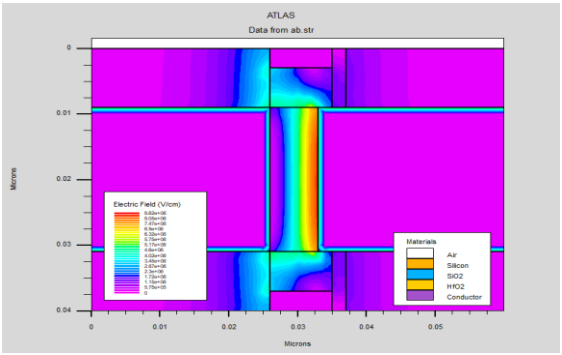

Figure 3. Electric field distribution of proposed device

The simulation work is carried out with three different drain doping concentrations (Nd = 1×10^{18} cm^{-3}, 2×10^{18} cm^{-3}, and 3×10^{19} cm^{-3}) for the proposed device. Table 1 presents the values of the gate work function, gate-on-drain overlap work function, and equivalent oxide thickness beneath the gate-on-drain

overlap for each of these drain doping concentrations (23). The channel length for all structures was set at 10 nanometers. The same gate work functions were utilized in the remaining three configurations. In these proposed structures, the selected a gate-on-drain overlap length of

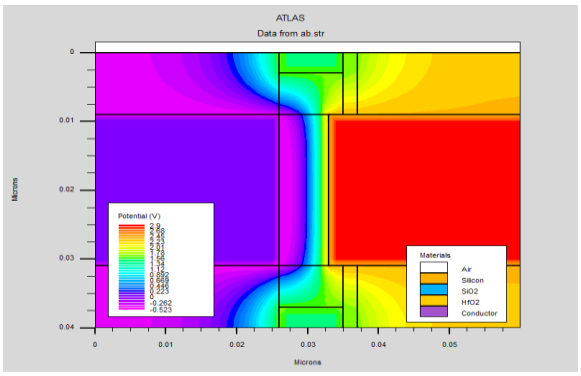

Figure 4. Potential distribution of proposed device

TABLE 1. Parameter used for the simulation proposed device

Used Parameter	DMG-ODS-TFET
Device Length (W_L)	60 nm
Gate Length (L_G)	10 nm
Source Length (L_S)	25nm
Drain Length (L_D)	25nm
Channel Length (L_C)	10nm
Doping of Source (D_S)	$1x10^{20}$ cm^{-3}
Doping of Drain (D_D)	$1x10^{18}$ cm^{-3}
Doping of Channel (D_C)	$1x10^{17}$ cm^{-3}
Metal Gate Work Function (W_F)	4.8eV

20 nm, which was found to be optimal for reducing ambipolar current in DMG-OD-TFET (24). Importantly, the introduction of the gate-on-drain overlap did not have an adverse impact on the AC performance of the device through increased gate-drain capacitance.

The on state current and off state current for different doping concentrations are summarized in Tables 2, 3 and 4.

3. RESULTS AND DISCUSSION

The drain current (Id) versus gate-to-source voltage (Vgs) characteristics for a proposed device, investigating

TABLE 2. On current and off current at Nd= 1×10^{18} cm^{-3}

Gate Length	**Ion**(A/μm)	**Ioff**(A/μm)	Ion/Ioff
L=22nm	$4.2174e^{-6}$	$1.08069e^{-17}$	$3.90247e^{+11}$
L=18nm	$1.514e^{-5}$	$1.00242e^{-17}$	$1.51032e^{+12}$
L=14nm	$5.435e^{-5}$	$1.08069e^{-17}$	$5.02921e^{+12}$
L=12nm	$8.1414e^{-5}$	$9.21128e^{-18}$	$8.83853Ee^{+12}$
L=10nm	$8.1618e^{-4}$	$9.21128e^{-18}$	$4.9189e^{+14}$

TABLE 3. On current and off current at Nd= 2×10^{18} cm^{-3}

Gate Length	Ion(A/μm)	Ioff(A/μm)	Ion/Ioff
L=22nm	$4.1233e^{-5}$	$4.98288e^{-19}$	$8.27504e^{+13}$
L=18nm	$6.4603e^{-5}$	$2.24135e^{-18}$	$2.88231e^{+13}$
L=14nm	$7.1246e^{-5}$	$1.01878e^{-17}$	$1.54046e^{+13}$
L=12nm	$8.9812e^{-5}$	$6.67237\ e^{-15}$	$2.68791e^{+13}$
L=10nm	$6.1735e^{-4}$	$2.15899\ e^{-9}$	$2.98498e^{+13}$

TABLE 4. On current and off current at Nd= 3×10^{18} cm^{-3}

Gate Length	Ion(A/μm)	Ioff(A/μm)	Ion/Ioff
L=22nm	$4.0162e^{-6}$	$1.00224e^{-18}$	$4.00719e^{+13}$
L=18nm	$7.9799\ e^{-6}$	$2.20201e^{-17}$	$3.62393e^{+11}$
L=14nm	$1.0376e^{-6}$	$5.45632e^{-14}$	$3.74891e^{+11}$
L=12nm	$9.4744e^{-6}$	$3.87088e^{-14}$	$3.98756e^{+11}$
L=10nm	$9.4892e^{-6}$	$1.1615e^{-9}$	$2.12042e^{+11}$

the behavior of this proposed transistor under different operating conditions (25). The dual metal gate overlap on the drain (DMG-OD) side can help to reduce the tunneling barrier and improve electron injection from the source to the channel (26). This can lead to a higher on-state current (Ion) compared to traditional TFET designs. Consequently, the Id and Vgs curve should show an increased current level for a given Vgs, indicating improved device performance in the on-state (27). While DMG overlap can enhance gate control i.e. impact on gate leakage. Any unintended leakage current through the gate can affect the device's off-state performance. Depending on the materials and fabrication used, there may be variations in gate leakage current that are reflected in Figure 5.

The proposed device ability to achieve subthreshold swings below 60 mV/decade compared to conventional MOSFETs (28). With a DMG-OD side, the improvement in the subthreshold swing is due to enhanced gate control over the channel. A steeper subthreshold slope indicates better performance in the subthreshold region (29). The DMG structure allows for more precise control over the threshold voltage (Vth). By adjusting the work function of the metals or the gate length, can tune the Vth to this specific design requirements (30). This can be observed in the Id vs. Vgs characteristics, with shifts in the threshold voltage for different device configurations. As with any semiconductor device, there are likely trade-offs associated with this design. For instance, the overlap of the gate on the drain side may affect other device parameters such as transconductance, drain conductance, off state leakage current and lower breakdown voltage. The proposed device exhibits temperature-sensitive behavior due to the tunneling mechanism. The Id and Vgs characteristics of the proposed device is analyzed at different temperatures to understand how the DMG overlap on drain side will show and influences the device's temperature dependence as shown in Figure 6.

The proposed device is validated and analyzed with potential equations as shown in Equations 1-3.

To achieve the highest drain current for both the conventional device and the proposed structure when the gate voltage is at zero, they should operate in depletion mode. Consequently, in the 10nm technology, the maximum current for the proposed device occurs when VG=0. Notably, the drain current experiences a significant increase as the drain voltage varies while the gate voltage is held at zero. In TFET, the upper region of the channel needs to be depleted due to the gate channel bias. This depletion results in the movement of carriers towards the bottom of the channel, which in turn leads to the flow of drain current. As a result, the drain current predominantly flows in the lower area of the channel. This proposed device is expected to exhibit maximum velocity, the highest electron density, an effective

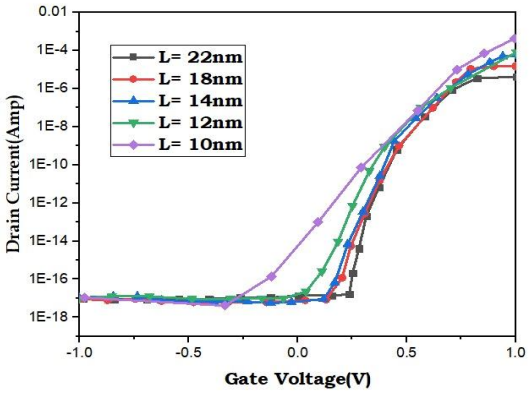

Figure 5. Drain current with gate voltage of proposed device at doping concentration Nd= 1×10^{18} cm^{-3}

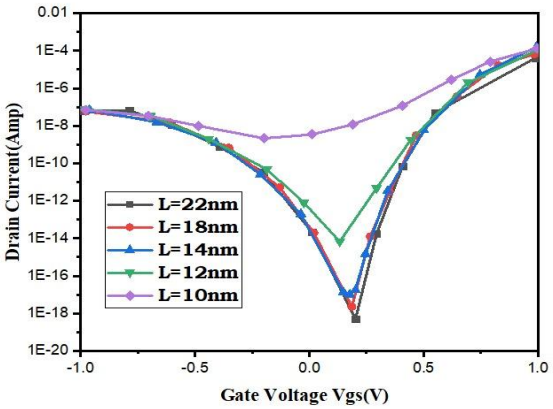

Figure 6. Drain current with gate voltage of proposed device at doping concentration Nd= 2×10^{18} cm^{-3}

channel depth, and improved drain current flow as shown in Figure 7.

$$f_T = \frac{g_m}{2\Pi(Cgs + Cgd)} \quad (1)$$

$$f_T = \frac{g_m}{2\Pi Cgg} \quad (2)$$

where Cgs -Gate to source capacitance

Cgd -Gate to drain capacitance

Cgg -Total gate capacitance

In the subthreshold region, drain conductance and drain voltage exhibits a steep increase in conductance with increasing drain voltage. This behavior signifies the proposed device ability to achieve a low subthreshold swing. In the saturation region, drain conductance may rapid continues to increase but gradually increase with increasing drain voltage. This is indicative of the device's ability to maintain a controlled and stable on-state current, which is essential for various applications. The DMG-OD side influences the drain conductance. It may affect the electric field distribution, gate control, and tunneling mechanism, all of which can directly impact conductance. The proposed TFET should exhibits a subthreshold swing and its performance significantly below the 60 mV/decade limit seen in traditional MOSFETs. Analyzing drain conductance for a proposed device is essential for understanding its electrical behavior, subthreshold characteristics, temperature sensitivity, radio frequency and overall suitability for various applications. Experimental measurements and device simulations are crucial for obtaining real-world data and validating the expected behavior of the device as shown in Figure 8.

$$I_d = zb(x)qn(x)v(x) \quad (3)$$

where z= channel width
b(x)=effective depth of the channel
q=electron charge
n(x)=electron density
v(x)=electron velocity

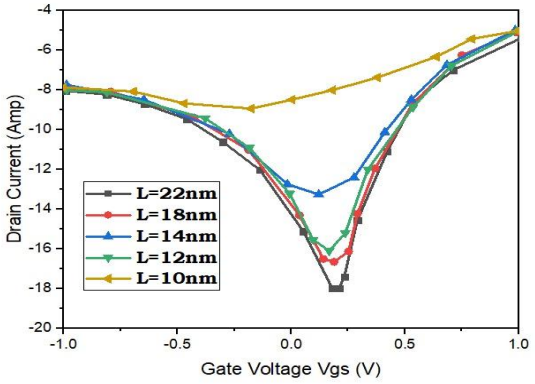

Figure 7. Drain current with a gate voltage of proposed device at doping concentration Nd= 3×10^{18} cm^{-3}

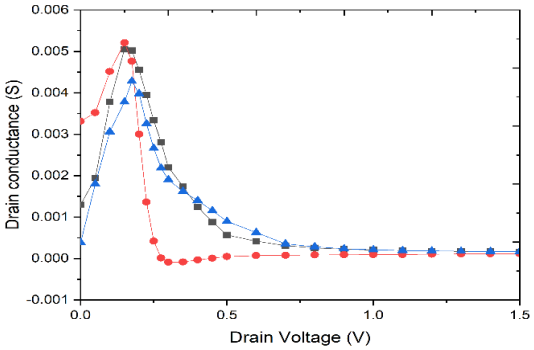

Figure 8. Drain conductance with a drain voltage of proposed device

The performance characteristics of different devices are evaluated in comparison to the proposed structure, as presented in Table 5. According to the comparison results, the proposed device exhibits and shows enhanced performance parameters when compared to existing devices and Table 6 shows the existing device

In semiconductor technology, TFETs are an advanced transistor designed to operate at lower power consumption compared to traditional MOSFETs. The dual metal gate overlap on the drain side to a feature in the TFET design that influences its performance.

TABLE 5. Performance Parameters Comparison comparison

Parameters	C TFET	SG TFET	DG TFET	HD-DG TFET	HD-DMG-TFET	DMG-OD-TEFT (18nm)	DMG-OD-TEFT (12nm)	DMG-OD-TEFT (10nm)
Ion(A/μm)	3.12	3.94	4.3	4.6	8.01	8.1	8.12	9.48
Ioff(A/μm)	$9.40e^{-11}$	$8.99e^{-11}$	$4.50\ e^{-11}$	$4.22e^{-11}$	1.34	1.12	1.14	1.16
Ion/Ioff	1.69	1.70	1.88	1.84	1.9	2.1	2.11	2.12
Gm(S/mm)	1.34	1.38	1.42	1.46	1.41	1.55	1.88	3.1
Gd(S/mm)	0.32	0.39	0.419	0.45	0.452	0.46	0.61	0.71
Ron(Ωmm)	1.41	1.61	1.32	0.88	0.6	0.71	0.72	0.51

TABLE 6. Comparision with existed devices

Parameters	C TFET	SG TFET	DG TFET	HD-DG TFET	Proposed device
Ion(A/μm)	2.12	2.9	3.1	4.5	6.78
Ioff(A/μm)	9.01	8.08	7.6	7.58	7.55
Ion/Ioff	2.12	1.07	1.6	1.72	3.21

possibly affecting the current leakage and switching speed. To improve or fill gaps in the design of a proposed TFET, experimenting with different semiconductor materials and metal combinations for the gates can significantly impact the device's performance. Novel materials may offer improved electrical characteristics, better control over the tunneling process and reduced leakage. The optimization of the gate dielectric material can affect the tunneling characteristics and overall transistor behavior. Innovations in dielectric materials may help in reducing leakage currents and enhancing device performance. Fine-tuning the manufacturing processes, such as the deposition and etching techniques, can improve the precision and quality of the Dual Metal Gate Overlap. Optimizing these processes can enhance the transistor's reliability and performance. Advanced computer modeling and simulation techniques can help researchers understand the behavior of the TFET at a fundamental level. This understanding can guide the refinement of the Dual Metal Gate Overlap design.

The proposed device demonstrates superior drain conductance associated with the use of HfO_2 and SiO_2 dielectric materials. This elevated drain conductance plays a pivotal role in enabling the device to attain the highest packing density, primarily due to the augmented current flow within the device. As a result, the structural advantage inherent in the proposed device leads to a significant enhancement in advanced transconductance characteristics. A robust transconductance is crucial for achieving optimal device gain. However, the pursuit of reducing the subthreshold slope, though desirable, introduces a trade-off by causing an upturn in off-current and power dissipation within the device.

4. CONCLUSION

In this work, a Dual Metal Gate (DMG) Overlap on Drain Side Tunneling Field Effect Transistor (TFET) with spacer technique is investigated in 10nm technology. This proposed device achieving the highest drain current at zero gate voltage, while operating in depletion mode, is crucial for optimizing the proposed device functionality. HfO_2 holds significant potential as a semiconductor material for high-voltage and high-frequency applications, including cosmic cells and energy devices. In this work, the design, analysis and calculation of performance parameters of both DC and RF properties, for a unique advanced device designed for the 10nm technology node using Silvaco TCAD. The proposed structure, utilizing Silvaco TCAD in the context of 10nm innovations, enhances various electrical properties such as on current (Ion), off current (Ioff), Ion/Ioff ratio, as well as RF properties including drain conductance (Gd) and on-resistance (Ron). The main analysis presented in this article demonstrates the ability to achieve exceptional performance in the proposed structure. This device incorporates a hetero-junction created by merging silicon materials with hafnium oxide at the drain-channel junction. Furthermore, it employs a hetero-dielectric gate stack consisting of SiO_2 and HfO_2, with HfO_2 dielectric showing significant potential as a semiconductor material for applications requiring high voltage and high frequency range. These findings include maintaining an average subthreshold swing of this proposed device is less than 60 mV/dec (approximately 45 mV/dec), achieving a low OFF-state current of around 10^{-09}A/μm, and attaining an impressive ION/IOFF ratio of approximately 10^{11}, even when using high drain doping concentrations up to $N_D = 3 \times 10^{18}$ cm^{-3}. These results provide strong motivation for researchers to pursue experimental implementations of TFETs with enhanced performance. As a result, this advanced structure is well-suited for high-frequency applications.

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Persian Abstract

چکیده

این مقاله به بررسی رفتار الکتریکی و عملکرد یک همپوشانی دروازه فلزی دوگانه روی ترانزیستور اثر میدان تونل سمت تخلیه با Spacer (DMG-ODS-TFET) در فناوری ۱۰ نانومتری می‌پردازد. در این طرح، استفاده از دو فلز مختلف برای ایجاد گیت، الکترواستاتیک را به طور موثر حفظ می کند و جریان نشتی گیت را به حداقل می رساند. این ساختار توسط دی اکسید سیلیکون و اکسید هافنیوم به عنوان مواد دی الکتریک تشکیل شده است. ویژگی‌های جریان تخلیه مانند نوسان زیرآستانه، جریان در حالت، جریان نشتی خارج از حالت، و رسانایی برای دستگاه پیشنهادی با استفاده از ابزار شبیه‌ساز دستگاه عددی دو بعدی موجود silvaco محاسبه می‌شود. ویژگی های دستگاه پیشنهادی با تغییر در طول کانال، غلظت دوپینگ درین و منبع، و ضخامت لایه اکسید متفاوت است. این ساختار جریان خاموش کمتر و نسبت جریان روشن به خاموش بهتر با جریان تخلیه بهبود یافته را نشان می دهد. در نتیجه، طرح پیشنهادی به طور موثر کنترل گیت و جریان نشتی را متعادل می‌کند و در نتیجه نسبت به دستگاه‌های دروازه فلزی معمولی و دوگانه برتری دارد. بر اساس پارامترهای عملکرد بهبود یافته، این ساختار پیشنهادی برای کاربردهای فرکانس بالا مناسب است.