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Design and Analysis of Hetero Dielectric Dual Material Gate Underlap Spacer Tunnel Field Effect Transistor

S. Howldar, B. Balaji*, K. Srinivasa Rao

Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Green Fields, Vaddeswaram, Andhra, India

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ABSTRACT

This paper presents a design and analysis of a Hetero Dielectric Dual Material Gate Underlap Spacer Tunnel Field Effect Transistor, aiming to enhance device performance and overcome inherent limitations. The proposed design incorporates a hetero dielectric gate stack, which consists of two distinct dielectric materials such as high-k-dielectric material as hafnium oxide (HfO_2) and low-k dielectric material as silicon dioxide (SiO_2). With different permittivity values. By selecting these materials, the gate stack can effectively modulate the electric field distribution within the device, improving electrostatic control and reducing ambipolar conduction. Furthermore, an underlap spacer is introduced in the presented structure to create a physical separation between the source and the channel regions. This spacer helps in reducing the direct source-to-drain tunneling current, enhancing the Ion/Ioff current ratio and reducing the subthreshold swing. Additionally, the underlap spacer enables improved gate control over the tunneling process. The proposed Tunnel Field Effect Transistor design is thoroughly analyzed using numerical simulations based on the technology computer-aided design (TCAD) simulator. Performance metrics as the on-state current (Ion), the off-state current (Ioff), ION/IOFF ratio, drain conductance (Gd) and transconductance (Gm) to assess the device's performance. Therefore, these improvements contribute to lower power consumption and improved circuit performance, making it a promising device for low-power applications.

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NOMENCLATURE

HfO_2	Hafnium oxide	Si	Silicon
SiO_2	Silicon dioxide	Ion	On state current
Ioff	Off state current	G_d	Drain conductance
Gm	Transconductance	I_d	Drain Current
Vgs	Gate to source voltage	V_{ds}	Drain to source voltage

1. INTRODUCTION

In recent years, the constant demand for faster and more energy-efficient electronic devices has led to the exploration of novel transistor designs. Traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) have been the cornerstone of the semiconductor industry for several decades. The MOSFET is a fundamental electronic device that forms the building block of modern integrated circuits (ICs) [1]. It is a type of field-effect transistor that relies on the modulation of an electric field to control the flow of current. MOSFETs are widely used in various electronic devices Such as computers smartphones, power amplifiers and memory chips. However, their performance improvements have encountered significant challenges in recent years, primarily due to limitations related to power consumption and leakage current [2].

TFET is an emerging transistor technology that aims to overcome certain limitations of MOSFETs, particularly in terms of power consumption and subthreshold leakage [3, 4]. TFETs operate based on the

*Corresponding Author Email: vahividi@gmail.com (B. Balaji)

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principle of quantum tunneling, where charge carriers (typically electrons) can pass through a thin barrier without requiring high energy. In TFETs, the conducting channel is replaced by a thin insulating barrier (tunneling junction) between the source and drain terminals. By applying a voltage to the gate terminal, a strong electric field is created across the barrier, facilitating quantum tunneling of carriers from the source to the drain. This tunneling mechanism enables TFETs to achieve lower threshold voltages and potentially reduce power consumption compared to MOSFETs [5].

TFET hold promise for low power applications and are actively researched to improve their performance and overcome challenges related to switching speed, on/off current ratio, and manufacturing scalability. However, TFET technology is still in the early stages of development, and practical implementation and widespread adoption are yet to be realized [6].

Dual material Gate TFET is a variation of TFET design that incorporates two different materials in the gate structure such as high-k dielectric material as hafnium oxide (HfO_2) and low-k dielectric material as silicon dioxide (SiO_2) instead of using a single material [7]. The use of distinct materials in the gate region allows for enhanced control over the transistor's behavior and provides unique performance benefits. Dual Material Gate TFETs have gained attention as a potential solution for achieving improved performance and energy efficiency [8].

The operation of dual material TFET is based on the principle of quantum band to band tunneling (BTBT), where charge carriers pass through a thin barrier to control the flow of current. By utilizing two different materials in the gate structure, the transistor's characteristics can be tailored to achieve desired performance metrics [9].

In this paper, we have designed a advanced Hetero Dielectric Dual Material Gate Underlap Spacer TFET, to overcome the limitations of conventional TFET designs and further to improve device performance parameters in submicron technology. The key components of this design include a hetero dielectric gate stack and an underlap spacer [10, 11]. The hetero dielectric gate stack involves the use of two different dielectric materials such as high-k dielectric material as hafnium oxide (HfO_2) and low-k dielectric material as silicon dioxide (SiO_2) [12]. By selecting these dielectric materials in the proposed structure the electric field distribution leading to enhanced electrostatic control. This improved control helps to reduce ambipolar conduction, a significant challenge in TFETs, and allows for efficient modulation of the device's on/off characteristics [13].

In addition to the hetero dielectric gate stack, we have incorporated an underlap spacer in the TFET structure. The underlap spacer creates a physical separation between the source and the channel regions. This separation plays a vital role in reducing the direct source-to-drain tunneling current, which is a major contributor to off-state leakage in TFETs [14]. By minimizing this leakage current, the underlap spacer improves the on/off current ratio and enhances the overall performance of the device.The combination of the hetero dielectric gate stack and the underlap spacer offers significant advantages for TFET performance. However, it requires a comprehensive analysis to understand the impact of these design modifications on various device metrics. Therefore, in this work, we used technology computer-aided design (TCAD) framework to evaluate the performance of the proposed device [15].

The advantages of this model have the significantly reduce leakage current, leading to improved energy efficiency, making them valuable for low power and provide better performance leading to high performance integrated circuits. It could align with the trend of increasing transistor density, which is crucial for advanced semiconductor technology.

The disadvantages of this Design increase the complexity of the fabrication process, higher production costs under various operating conditions and manufacturing variations is essential for real-world applications. Developing comprehensive testing methods for the new design to verify its performance, reliability, and compatibility can be a complex and time-consuming task.

In this paper the proposed device and utilized parameters are presented in second section. The result and discussions are presented in third section. The final section presented with conclusion.

2. STRUCTURE OF PROPOSED DEVICE

The proposed TFET device made of high-k and low-k dielectric materials and is responsible for the tunneling of charge carriers. The gate stack of the TFET incorporates a hetero dielectric material composition. It consists of two distinct dielectric materials such as high-k dielectric material as hafnium oxide (HfO_2) and low-k dielectric material as silicon dioxide (SiO_2). The choice of these materials is critical as it influences the electric field distribution and the tunneling behavior within the device. To enhance the device's performance, an underlap spacer is introduced between the source and channel regions. This spacer physically separates the two regions, reducing direct source-to-drain tunneling current [16].

In the proposed structure different work functions are used to optimize the tunneling characteristics of the HD-DMG-US TFET. By carefully selecting the materials for the source, channel, and drain regions, the bandgap can be tailored to facilitate efficient tunneling. The band gap engineering ensures a favorable alignment of the band edges between the source and channel regions. This alignment promotes efficient carrier tunneling through the tunneling barrier while minimizing leakage current

when the device is in the off-state [17]. Figure 1 shows the conventional TFET utilized high-k dielectric material being hafnium oxide (HfO_2) and low-k dielectric material as silicon dioxide (SiO_2) and silicon(Si).The HD-DMG-US TFET device dimensions of 60 nm, channel length of 5nm, source length of 27.5 nm, drain length of 27.5 nm.A gate is connected to the Silicon Dioxide (SiO_2) material at top and second gate connected to Silicon Dioxide (SiO_2) at the bottom [18]. Figure 2 shows the structure of Dual Material Gate TFETs where the, materials such as high-k and low-k dielectrics and Silicon (Si) are utilized for implementation [19].

Figure 3 shows the HfO_2 Spacer Tunnel FETs .The material utilised for the spacer in the device is HfO_2, and the same high-k dielectric material employed in four spots. Figure 4 shows the Hetero – Dielectirc Dual Material Gate Tunnel FET(HD-DMG-TFET) consists of two dielectric materials at the top and bottom under the gate such as high-k dielectric material as hafnium oxide (HfO_2) and low-k dielectric material as silicon dioxide (SiO_2),where SiO_2 acts as an interfacial layer between HfO_2 and the silicon channel region [20, 21]. This interface layer improves contact between the semiconductor and the HfO_2 and lowers the risk of defect development at the contact. The proposed Underlap Spacer Dielectric Tunnel FET(USD-TFET) as shown in Figure 5 can increase the channel resistance and induce ON-state current degradation [22].

The potential improvement of proposed structur could lead to more energy-efficient and have high-performance metrics such as on-state current, subthreshold slope (SS), and transconductance (gm).

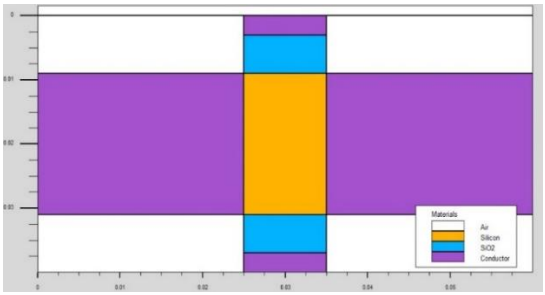

Figure 1. Two Dimensional View of Coventional TFET

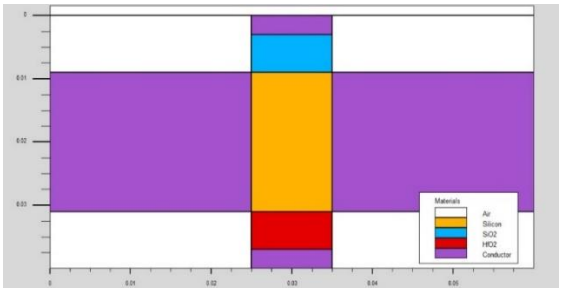

Figure 2. Two Dimensional View of Dual Material Gate TFET

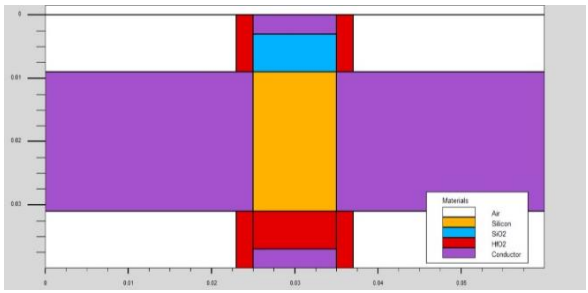

Figure 3. Two Dimensional View of HfO2 Spacer Tunnel TFET

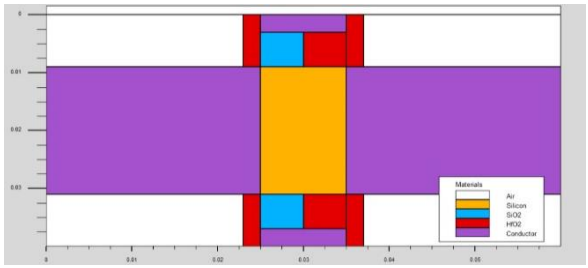

Figure 4. Two Dimensional View of Hetero Dielectric – Dual Material Gate Tunnel FET

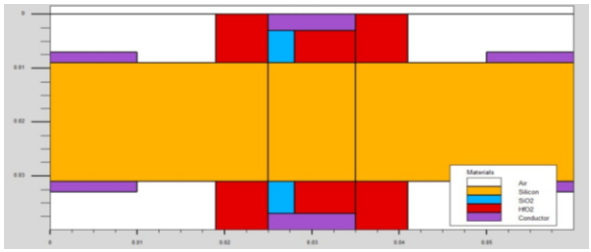

Figure 5. Proposed HD-DMG-US Tunnel FET

Innovative gate engineering techniques and materials are used to achieve lower subthreshold swing and reduced leakage current and performance calulated in nanotechnology. The Hetero Dielectric-DM-US TFET may be adaptable to advanced semiconductor fabrication processes and could be scaled down for future technology nodes, aligning with trends in nanoelectronics.

The HD-DMG-US TFET device utilized the different parameters for simulation as shown in Tables 1, 2 and 3. Table 4 shows the values of Ion and Ioff current, for different structures and different spacer length.

3. THE NOVALITY OF THE PROPOSED MODEL

3. 1. Hetero Dielectric Gate The hetero dielectric refers to the use of different materials for the gate insulator in different regions of the transistor. This allows for more precise control of the electric field, which can impact the transistor's performance characteristics, such as the subthreshold swing and on-state curren.

TABLE 1. Parameter used for the proposed TFET

Parameter	HD-DMG-US TFET
Device Length (W_L)	60 nm
Gate Length (L_G)	5 nm
Source Length (L_S)	27.5nm
Drain Length (L_D)	27.5nm
Channel Length (L_C)	5nm
Doping of Source (D_S)	$1x10^{17}$ cm^{-3}
Doping of Drain (D_D)	$1x10^{18}$ cm^{-3}
Doping of Channel (D_C)	$1x10^{20}$ cm^{-3}
Metal Gate Work Function (W_F)	4.8eV
Thickness of SiO_2	2nm
Thickness of HfO_2	3nm

TABLE 2. On-state and Off state currents for various TFET

TFET Architecture	IOFF	ION	ION
C-TFET	1.33E-10	4.01E-05	2.82E+05
DMG-TFET	2.10E-11	3.50E-05	3.13E+05
S-TFET	2.30E-11	3.48E-05	1.46E+06
HD-DMG-TFET	3.30E-11	3.21E-05	4.32E+07
Proposed Device	5.20E-11	2.05E-05	6.33E+07

TABLE 3. On-state and Off-state currents for different spacer length

Gate Length (nm)	I_{OFF}	I_{ON}	I_{ON}/I_{OFF}
5nm	5.10E-12	4.13E-05	5.50E+07
10nm	3.12E-11	4.70E-05	3.20E+06
15nm	2.12E-11	5.20E-05	2.50E+06

TABLE 4. On-state and Off-state currents for doping concentrations

HD-DMG-TFET	I_{OFF}	I_{ON}	I_{ON}/I_{OFF}
$1x10^{17}$ cm^{-3} - Source	1.20E-11	3.35E-05	2.50E+06
$1x10^{18}$ cm^{-3} - Drain	2.10E-11	3.25E-05	3.02E+06
$1x10^{20}$ cm^{-3} -Channel	4.15E-11	3.15E-05	4.50E+07

3. 2. Dual Material Gate The dual material gate indicates that the gate electrode, which controls the flow of current in the transistor, is composed of two distinct materials with different properties. This design can help optimize the transistor's electrostatics and enhance its switching performance.

3. 3. Underlap Spacer The underlap spacer material placed between the source and drain regions. This spacer serves multiple purposes, including reducing the direct source-to-drain tunneling current and improving the overall transistor performance.

4. RESULTS AND DISCUSSIONS

4. 1. Drain Current Characteristics The Id Vs Vgs characteristics represent the drain current (Id) as a function of the gate-to-source voltage (Vgs). These characteristics provide insights into the transistor's behavior and its operating region. Figure 6 shows the characteristics of designed HD-DMG US TFET results are compared with C-TFET,DMG-TFET,S-TFET and HD-DMG-TFET. It can be seen that HD-DMG-US TFET exhibits much improved ON current compared to other devices. This is possible by the hetero dielectric materials such as high-k dielectric material as hafnium oxide (HfO_2) and low-k dielectric material as silicon dioxide (SiO_2).Due to heterojunction and dielectric materials lead to increase in the tunneling volume and due to the barrier width reduction [23]. The proposed device is much better than other devices because it uses materials with a lower energy threshold, has a special junction (heterojunction), and includes Hafnium Oxide (HfO_2) near where the electrical current flows (source-channel interface). These factors together allow more electrons to move through the device, and they also prevent a certain type of switching (ambipolar switching) at another interface (drain interface). This is achieved by applying a specific type of doping called Gaussian doping, which expands the depleted region where the current flows (drain-channel interface.

The I_d Vs V_{ds} characteristics of USD-TFET with different types of materials such as Hafnium Oxide (HfO_2), Silicon(Si), and Silicon Dioxide (SiO_2) [24], are found in this construction. The drain current of USD-TFET increased when compared to the other devices as shown in Figure 7.

The diagram illustrates the design of the proposed device, featuring two gates with distinct workfunctions (φ1 and φ2) for the tunnel gate, control gate, and auxiliary gates. By keeping the workfunctions of the tunnel gate and auxiliary gate constant (φ1 and φ3) and adjusting the workfunction of the control gate (φ2), we can achieve the most efficient switching currents for the specific hetero combination [25].

We compared the DC performance of the HD-DMG-US TFET with a conventional device using dielectric materials. The influence of the source dielectric on the drain current with gate-source voltage (VGS) is depicted. We noticed a higher on-current (Ion) in the HD-DMG-US TFET, primarily attributed to reduced tunneling barriers at the junction, improved subthreshold slope, and a higher Ion/Ioff ratio. These characteristics make the HD-DMG-US TFET structure well-suited for low-power applications [26].

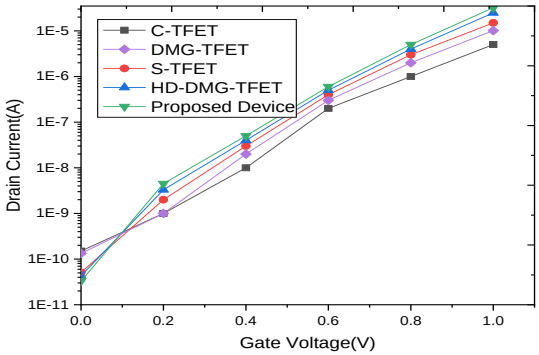

Figure 6. Comparision of Id vs Vgs Characteristics HD-DMG-US TFET with other devices

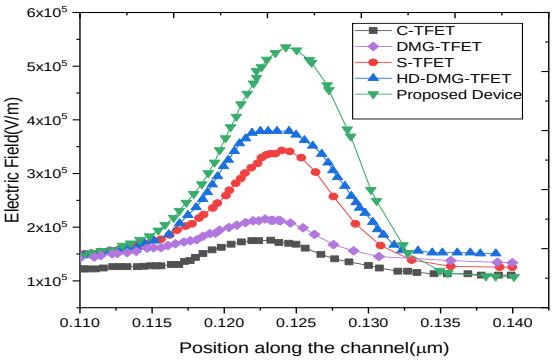

Figure 8. Electric field Comparision of HD-DMG- US TFET with other devices

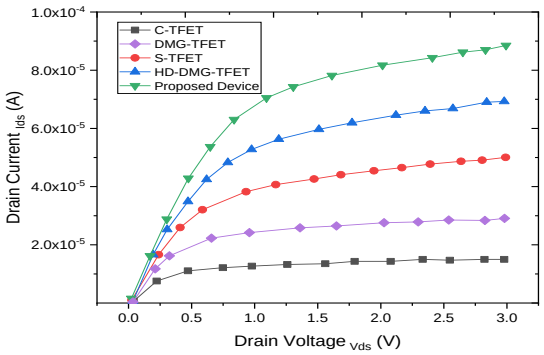

Figure 7. Comparision of Id vs Vds Characteristics HD-DMG-US TFET with other devices

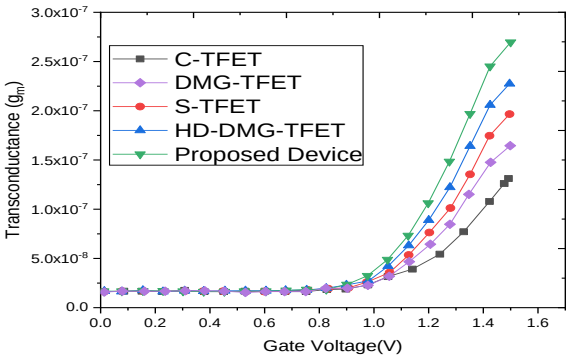

Figure 9. Transconductance Comparision of HD-DMG- US TFET with other devices

Cavity formation expands as the barrier width between the valence and conduction bands increases, indicating reduced electron tunneling. Consequently, the current conduction is diminished. Furthermore, when varying the cavity length, it was observed that the drain current (Id) at Vds = 1.0 V is significantly lower compared to Vds = 0.5 V. Hence, it becomes apparent that the HD-DMG-US-TFET with the gate underlap technique demonstrates the principle of tunneling.

Figure 8 shows the electric field distribution of proposed devices such as Underlap Spacer Dielectric Tunnel FET(USD-TFET), HD-DMG-TFET, Conventional-Tunnel FET, Dual Material Gate-Tunnel FET(DMG-TFET) and HfO_2 Spacer Tunnel FET(S-TFET) Devices.

4. 2. Analog Characteristics Figure 9 shows transconductance(gm/Ids) of HD-DMG-US TFET comparision with Conventional-Tunnel FET, Dual Material Gate-Tunnel FET(DMG-US TFET) and HfO2 Spacer Tunnel FET(S-TFET) [27, 28]. The devices that turn on at higher voltages (threshold voltages) have low gm/Ids values. Higher gm/Ids values are obtained when the devices are OFF (Vth). Electrically doped devices turn on at a lower voltage than conventionally doped devices, resulting in high gm/Ids for HD-DMG US TFET [29].

Figure 10 shows drain conductance of proposed device as a function of drain voltage for different structures.The drain ON (ION) and OFF (IOFF) currents as a function of device temperature [30, 31]. These findings revealed that the ON drain current increases linearly as temperature rises, whereas the drain OFF current rises exponentially as temperature rises. The primary electrical factors that govern the transistor's properties in analogue or digital circuits, such as ION /IOFF ratio, drain induced barrier lowering (DIBL), and VT, are all affected by the transistor's working temperature dependent characteristics as shown in Figure 11 [32].

The evaluation of proposed design performs at smaller feature sizes, considering quantum mechanical effects and the potential for use in advanced technology nodes.Analyze the potential for improved energy efficiency in low-power applications, especially in scenarios where the TFET's unique tunneling mechanism provides advantages over traditional MOSFETs. Consider the device's reliability under

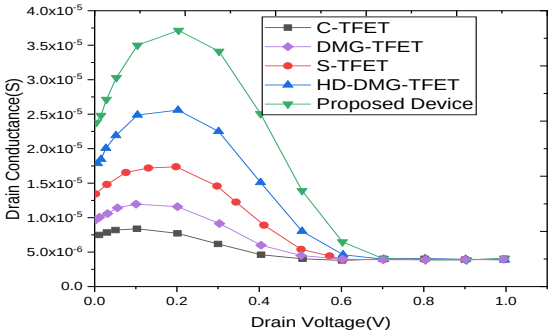

Figure 10. Drainconductance Comparision of HD-DMG-US TFET with other devices

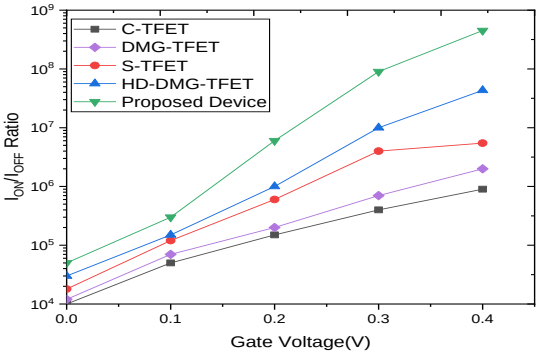

Figure 11. Ion/Ioff ratio Comparision of HD-DMG- US TFET with other devices

different operating conditions, stress, temperature, and process variability, and compare it to existing technologies [33].

5.CONCLUSION

The design and analysis of the Hetero Dielectric Dual Material Gate Underlap Spacer TFET offer significant advancements in the field of transistor technology and made of high-k dielectric material being hafnium oxide (HfO_2) and low-k dielectric material as silicon dioxide (SiO_2). The proposed device incorporates a hetero dielectric gate stack and an underlap spacer. It exhibited an improved on/off current ratio, reduced sub threshold swing, and enhanced gate control over the tunneling process. These improvements contribute to lower power consumption, increased switching efficiency, and better overall device performance. The underlap spacer played a crucial role in reducing off-state leakage current by physically separating the source and channel regions, while the hetero dielectric gate stack improved electrostatic control and minimized am bipolar conduction. The findings from this work highlight the potential of the Hetero Dielectric Dual Material Gate Underlap Spacer TFET for future low-power electronic applications. Further research can focus on exploring additional combinations of dielectric materials for the gate stack, optimizing band gap engineering, and investigating the device's behavior under different operating conditions. Continued advancements in TFET technology will contribute to meeting the growing demands of the semiconductor industry for energy-efficient electronic devices.

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Persian Abstract

چکیده

این مقاله طراحی و تجزیه و تحلیل یک ترانزیستور اثر میدانی تونل زیرلاپ تونل دوگانه گیت دو الکتریک هترو دی الکتریک را با هدف افزایش عملکرد دستگاه و غلبه بر محدودیت‌های ذاتی ارائه می‌کند. طرح پیشنهادی ترانزیستور اثر میدانی تونل شامل یک پشته دروازه دی الکتریک هترو است که از دو ماده دی الکتریک متمایز مانند مواد دی الکتریک بالا به عنوان اکسید هافنیوم (HfO_2) و مواد دی الکتریک کم k به عنوان دی اکسید سیلیکون (SiO_2) تشکیل شده است. با مقادیر گذردهی مختلف با انتخاب این مواد، پشته دروازه می تواند به طور موثر توزیع میدان الکتریکی را در دستگاه تعدیل کند، کنترل الکترواستاتیکی را بهبود بخشد و رسانش دوقطبی را کاهش دهد. علاوه بر این، یک فاصله دهنده زیرپوش در ساختار ترانزیستور اثر میدان تونل برای ایجاد یک جدایی فیزیکی بین منبع و مناطق کانال معرفی شده است. این اسپیسر به کاهش جریان مستقیم تونل منبع به تخلیه، افزایش نسبت جریان یون/آیوف و کاهش نوسان زیرآستانه کمک می کند. علاوه بر این، فاصله‌دهنده زیرپوش، کنترل دروازه‌ای را بر فرآیند تونل‌زنی بهبود می‌بخشد. طرح پیشنهادی ترانزیستور اثر میدانی تونل به طور کامل با استفاده از شبیه‌سازی‌های عددی مبتنی بر شبیه‌ساز طراحی به کمک رایانه (TCAD) تجزیه و تحلیل می‌شود. معیارهای عملکرد به عنوان جریان روشن (Ion)، جریان خارج از حالت (Ioff)، نسبت ION/IOFF، رسانایی تخلیه (Gd) و رسانایی ترانس (Gm) برای ارزیابی عملکرد دستگاه بررسی می‌گردد. بنابراین، این پیشرفت‌ها به مصرف انرژی کمتر و بهبود عملکرد مدار کمک می‌کند و آن را به دستگاهی امیدوارکننده برای کاربردهای کم مصرف تبدیل می‌کند.