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A Fault Tolerant Operation of 3-Phase, 5-Level CHBMLI under Open Circuit Fault Conditions

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A B S T R A C T

Fault detection and its restoration is the major challenge for the smooth functioning of the Multi-Level Inverter (MLI). In this paper, fault detection and its clearance scheme for an Open Circuit (OC) fault on a 3-level 5-level Cascaded H-Bridge Multi-Level Inverter (CHBMLI) has been developed and tested to improve the reliability and suitability of the system. An accurate and fast detection, isolation and bypassing of faulty bridges enhance the reliability, suitability, and acceptability of CHBMLI in any domestic, industrial drive applications. To reschedule the line voltage and current value close to the pre-fault level, a Neutral Point Shift (NPS) technique is presented in this paper. The desired output voltage is governed by Level Shift Pulse Width Modulation (LSPWM) technique. The proposed scheme is developed in MATLAB/Simulink environment and results are validated by using Opal-RT simulator. Simulation results has confirmed the performance and Opal-RT simulator results shows feasibility and applicability of the proposed scheme.

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NOMENCLATURE

A_{cr}	Peak value of triangular carrier signals	V_{AB}, V_{BC}, V_{CA}	Output line voltages
A_m	Peak value of modulating signals	$V_{\_Sa14}$	Instantaneous voltage across switch S_{a14}
f_{cr}	Frequency of carrier signals	i_A	Instantaneous phase-A current
f_m	Frequency of modulating signals	N	Load neutral point
n	Number of bridges	P_n	CHBMLI neutral point
A_1, A_2	Bridges H_1 and H_2 of phase-A	P_n'	Shifted neutral point of CHBMLI
B_1, B_2	Bridges H_1 and H_2 of phase-B	L_1, L_2, L_3	New phase voltages with NPS
C_1, C_2	Bridges H_1 and H_2 of phase-C	a	New line voltage with NPS
V_{dc}	Input DC supply to CHBMLI	θ_{cr}	Phase angle between triangular carrier
v_{H1}, v_{H2}	Instantaneous bridge output ac voltage	α, β, γ	New phase angles with NPS

1. INTRODUCTION

Multilevel Inverters (MLI) are widely accepted in all industrial, domestic, and electric power grid utility systems to improve the sustainability and reliability of the overall system [1]. Due to increasing penetration of renewable energy sources such as wind power and PV solar power, the importance of MLI has increased [2, 3]. The MLI has various advantages such as low voltage stress (dv/dt) across switches, low Total Harmonic Distortion (THD) of output ac voltages, low rating of IGBT switches and providing effective performance by conventional power electronics inverters [4, 5]. Because of their exclusive merits, the MLI is being used in various applications like v/f control in drive systems, HVDC transmission systems [6, 7]. Many topologies of MLI are available with different switch combinations and source arrangements. Some of the standard multilevel inverter topologies are further subclassified as: Flying Capacitors/Capacitor Clamped MLI (FCMLI), Neutral Point Clamped/Diode Clamped Multi-Level Inverter (NPCMLI), and Cascaded H-bridge MLI (CHBMLI), and their comparison is given in Table 1 [8, 9]. The CHBMLI is one of the most effective and popular

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topology. The advantage of CHBMLI is that, if any bridge is faulty, it bypasses the faulty bridge and provides continuous supply from other bridges. Since the CHBMLI requires separate DC sources, hence, it is suitable for several renewable energy sources like wind, PV, and fuel cells as shown in Figure 1. It is also suitable for medium voltage, high power distribution, Battery Energy Storage Systems (BESS), and industrial drives due to a high degree of modularity and high voltage ride-through [10, 11]. In CHBMLI, the number of levels in output voltage increases with an increase in the number of bridges. So, the reliability of the inverter depends on the number of components present in the system.

Due to the large number of semiconductors i.e., IGBT switches in MLI, the chances of failures in components increase which tends to create Open-Circuit (OC) and

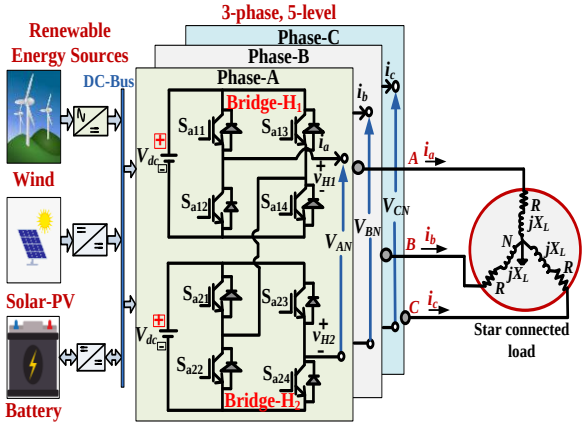

Figure 1. General block diagram of DC micro-grid with 3-phase, 5-level CHBMLI

TABLE 1. Comparative analysis of classical multilevel inverter

Sr. No.	Parameters	NPCMLI	FCMLI	CHBMLI
1	Output phase voltage levels for star connected load	m	m	m
2	Output voltage (line-line) levels	(2m-1)	(2m-1)	(2m-1)
3	Power semiconductor switches (3-ϕ)	6(m-1)	6(m-1)	6(m-1)
4	Clamping diodes (Independent)	3(m-1)(m-2)	0	0
5	DC bus capacitors	(m-1)	(m-1)	$\frac{3(m-1)}{2}$
6	Balancing capacitors	0	$\frac{3(m-1)(m-2)}{2}$	0
7	Voltage unbalancing problem	Average	High	Very low
8	Modularity	Less	Less	High
9	Asymmetrical input voltage configuration	Not possible	Not possible	Possible
10	Switching states of MLI in state space diagram including multiple states	m^3	m^3	m^3
11	Applications	Motor drive system, STATCOM	Motor drive system, STATCOM	Motor drive system, PV, fuel cells, BESS and grid integrated DG applications

Short-Circuit (SC) faults [12, 13]. The fault in the gate terminal in IGBT switches is considered as an OC fault. The switch fault count is approximately 1/3rd of the total fault in power converters. The OC fault in any switch of CHBMLI bridge leads to unbalanced load, and voltage disturbed. This creates unbalancing in output current and voltage, which increases the chances of other devices failure and may lead to the system collapse. The distribution of faults due to failure of components such as PCB 26%, capacitor 30%, semiconductor devices 21%, solder joint 13%, conductor 3%, and other 7% in power electronics converters is shown in Figure 2 [14]. In this paper, the comparative analysis of the OC fault detection methods, fault detection time, and their parameters are discussed. Sim et al. [15] detected the OC fault of CHBMLI based on output current waveform and zero voltage switching states, the detection time for identifying the faulty switch takes more than 40 msec. Here, the performance of detection is poor for faulty switch identification. The method presented by Faraz et al. [16] is based on a sliding mode observer to detect the

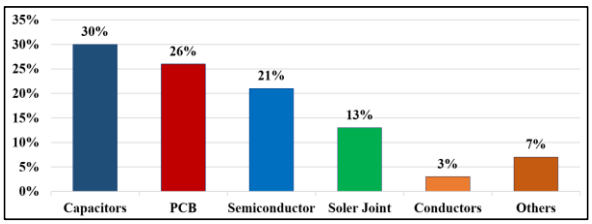

Figure 2. Faults percentages due to failure of devices in converters

OC faulty switch of a modular multilevel converter. The comparison is presented between each leg voltage and the voltage across the capacitor cell. It requires more than 100 msec to check each healthy bridge of the converter. In the fault detection method given by Anand et al. [17], the mean output bridge voltage is taken as detection parameter. The OC fault was detected for CHBMLI by comparing the half-cycle mean value of bridges voltage (HCMV) with normal operating mean output voltage. It can detect faulty switch of CHBMLI within 20 msec with LSPWM. The OC switch fault detection for T-Type MLI is given by He et al. [18]. In this method, the output current of MLI compares with online data which is already trained for OC fault in different conditions. This technique requires a set of data; due to this, it takes more than 20 msec for the execution of data for each healthy bridge. Thantirige et al. [19] presented the fault detection which is based on FFT analysis of phase current signal to detect faulty bridge. The fault is detected in less than 100 msec, this technique detects only faulty cell. This operation takes 60 msec to check the data in each step and this method also requires data training [20]. The accuracy is less under light load conditions. In the method given by Lezana et al. [21], fault detection is done based on output voltage switching frequency analysis for a cascaded multicell converter. The operation of fault detection is implemented by high frequency harmonic analysis. The behavior of fault is predicted under the approximate method. It takes more than 30 msec to implement this technique. A gravitational search algorithm is implemented to detect the OC fault for the cascaded half-bridge MLI [22]. This detection technique takes 20 msec for fault detection operation. It is for the limited number of switches and it does not give clear identification of faulty switches, since it is an approximate method. The generation of balanced three-phase line voltages and currents is described by Deepak and Das [23]. This is achieved by adjusting the three-phase angles with reference signals given to each leg of the inverter. The fault tolerance of MLI is implemented by the neutral point shift (NPS) technique to maximize the available voltage after bypassing the faulty bridge [24]. The fault is tolerated to improve overall system reliability. Research work is carried out in this concern to enhance the performance of the semiconductor switch with reliable operation. The main contributions of this paper are as follows:

- The developed algorithm based on instantaneous paramerters for fault detection and inherent isolation of the faulty bridge with minimum fault detection time.
- The neutral point shift (NPS) technique is implemented for fault-tolerant operation under OC faults on the switches to ensure uninterrupted, and reliable supply to the load.
- The proposed algorithm is implemented in MATLAB/Simulation and validated through the real-time simulator Opal-RT.

In section 2, the Cascaded H-bridge (CHB) 5-level inverter and PWM techniques are discussed. The analysis of fault detection and fault-tolerant NPS technique and OC fault detection in 3-phase, 5-level CHBMLI are addressed in section 3. Section 4 deals with the simulation results under different operating conditions. The Opal-RT simulator results are described in section 5. Conclusion of the proposed work is in section 6.

2. CASCADED H-BRIDGE 5-LEVEL INVERTER

The conventional power electronic inverters produce only two voltage levels either $+V_{dc}$ or $-V_{dc}$, but the CHBMLI generates an expected sinusoidal output voltage from several DC input voltage sources. It consists of a series connections of n-bridges. Each bridge gives three output voltage levels as $+V_{dc}$, 0, and $-V_{dc}$ obtained by implementing the different switching patterns [25]. The switching sequence and output voltages under normal operating condition is shown in Table 2. In symmetric cascaded H-bridge multilevel inverter, to get *m*-number of levels in output voltage, it requires 2*(*m*-1) switches, (*m*-1)/2 number of DC sources or number of H-bridges per phase leg, and switch blocking voltage is 2*(*m*-1) [26]. The sum of all the bridge output voltages gives the phase voltage. In this paper, for obtaining the 5-level, two H-bridges are connected in series in each phase as shown in Figure 1. i.e., ($V_{AN} = V_{H1} + V_{H2}$). The phase output voltages of MLI is given by:

$$\begin{cases} V_{AN} = m_{an} * n * V_{dc} \sin(\omega t) \\ V_{BN} = m_{bn} * n * V_{dc} \sin(\omega t - 120^0) \\ V_{CN} = m_{cn} * n * V_{dc} \sin(\omega t + 120^0) \end{cases} \quad (1)$$

The phase output magnitude with n-bridges;

$$\begin{cases} V_{ph} = m_{an} * n * V_{dc} \\ V_{line} = \sqrt{3} m_{an} * n * V_{dc} \end{cases} \quad (2)$$

The commonly used PWM techniques are Level Shift PWM (LSPWM) and Phase Shift PWM (PSPWM). These methods are simple and used in various topologies than space vector PWM. In LSPWM, all carrier signals have the same frequency and peak-to-peak amplitude. For an MLI with '*m*' voltage levels, (*m*-1) triangular carrier signals are required. The carrier signals are disposed over one another. In this paper, the level-shift pulse width modulation (LSPWM) technique is used to control the switching pattern to maintain the desired output voltage. The amplitude (m_a) and frequency (m_f) modulation index are given as,

$m_a = \frac{A_m}{A_{cr}(m-1)}$ and $m_f = \frac{f_{cr}}{f_m}$.

In PSPWM, the carrier signals are phase-shifted from one another, with the same frequency and peak-to-peak amplitude. An MLI with 'm' output voltage levels, (m-1) triangular carrier signals are required, whichare shifted by an angle (θ_{cr}). The comparison between PSPWM and LSPWM techniques is shown in Table 3.

$\theta_{cr} = \frac{360^0}{(m-1)}$, $m_a = \frac{A_m}{A_{cr}}$, and $m_f = \frac{f_{cr}}{f_m}$.

3. ANALYSIS OF FAULT DETECTION AND FAULT TOLERANT

Internal faults of the CHBMLI, such as the OC and SC faults are major faults. The internal short-circuit (SC) faults occur in IGBT, mainly due to the drastic increase in temperature. The peak current flows through collector to emitter of IGBT, without gate pulse, due to continuous increase in voltage beyond breakdown. The OC fault occurs due to open gate terminal or improper connection of collector and emitter terminal. In this paper, a fault detection algorithm is developed for 3-phase, 5-level CHBMLI to detect the fault under OC condition.

TABLE 2. Switching sequence and output voltage level of 5-levels CHBMLI

Sr. No.	Switching Combination	Output Voltage levels
1	S_{a11}, S_{a14}, S_{a21}, S_{a24}	$+2V_{dc}$
2	S_{a11}, S_{a14}, S_{a21}, S_{a22}	$+V_{dc}$
3	S_{a11}, S_{a14}, S_{a24}, S_{a23}	
4	S_{a11}, S_{a12}, S_{a21}, S_{a24}	
5	S_{a14}, S_{a13}, S_{a21}, S_{a24}	
6	S_{a11}, S_{a14}, S_{a23}, S_{a22}	
7	S_{a11}, S_{a12}, S_{a21}, S_{a22}	
8	S_{a11}, S_{a12}, S_{a24}, S_{a23}	0
9	S_{a14}, S_{a13}, S_{a21}, S_{a22}	
10	S_{a14}, S_{a13}, S_{a24}, S_{a23}	
11	S_{a13}, S_{a12}, S_{a21}, S_{a24}	
12	S_{a13}, S_{a12}, S_{a21}, S_{a22}	
13	S_{a13}, S_{a12}, S_{a24}, S_{a23}	$-V_{dc}$
14	S_{a11}, S_{a12}, S_{a23}, S_{a22}	
15	S_{a14}, S_{a13}, S_{a23}, S_{a22}	
16	S_{a13}, S_{a12}, S_{a23}, S_{a24}	$-2V_{dc}$

TABLE 3. Comparison between level-shift and phase-shift sinusoidal PWM

Parameters	Phase shift PWM	Level Shift PWM
Switching frequency (f_{sw} = f_{cr})	Same for all switches	Different
Conduction period (T)	Same for all switches	Different
Rotating of switching patterns	Not required	Required
Line-to-line voltage THD	Good	Better

3. 1. Open-Circuit (OC) Fault Detection

The open-circuit fault may occur on any switch, which creates an unbalance in the output voltages and currents. This leads to disturbance in the CHBMLI system. If the disturbance persists, the system will be shutdown. To avoid complete shutdown of the system, the algorithm proposed for fault detection and fault-tolerant techniques are implemented. An accurate and fast fault detection, inherent fault isolation, and bypassing of the faulty bridge ensure the reliability, suitability, and acceptability of CHBMLI in any domestic, industrial drive applications.

During OC fault, in any IGBT switch, the bridge voltage, current, and its magnitude deviates from normal operating condition with constant DC input. The fault detection in bridges is based on the monitoring of instantaneous bridge output voltage (v_{H1}, v_{H2}) and instantaneous output current (i_A). The faulty bridge, the faulty switch is identified by comparing the voltage across diagonal switches of each bridge and the instantaneous output current using fault detection algorithm. The proposed scheme for fault detection in 3-phase 5-level CHBMLI with fault-tolerant NPS technique is shown in Figure 3. For getting the optimality with minimum trade-off, all the possible OC fault conditions have been considered in the proposed

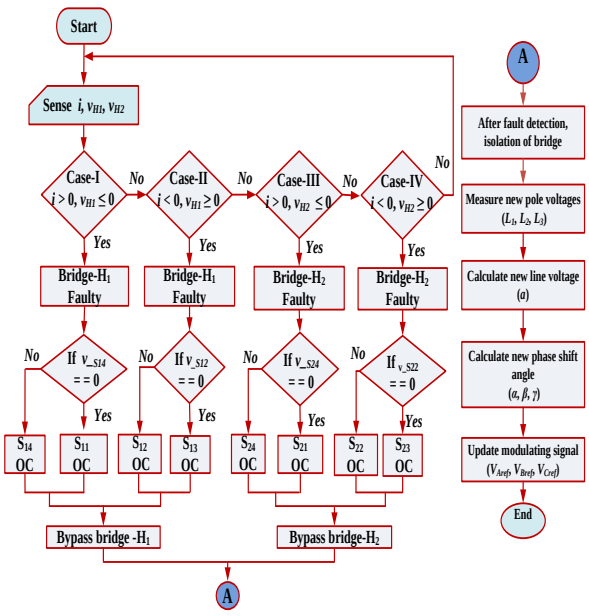

Figure 3. Flow chart for fault detection and fault tolerant with NPS

algorithm. The incorporation of NPS technique with the proposed algorithm shows promising results which are discussed in section 3. The fault detection algorithm provides a control signal to bypass the faulty bridge. Due to bypassing the faulty bridge, the output current and voltages become unbalanced, which is not acceptable for many applications. To make sure the output line currents and voltages are balanced after bypassing the faulty bridge, the NPS fault-tolerant control technique is implemented. To study the fault detection technique on different switches in open circuit fault, different cases are considered by misfiring the gate terminal.

The circuit diagrams, under OC fault conditions, for all the cases show the direction of current (i_A) and voltages (v_{H1}, v_{H2}) are depicted in Figures 4 to 7. The current direction is shown by a solid red line. The operation and switching sequence during OC fault in switch of 5-level CHBMLI is shown in Table 4. For example, if $v_{H1} \leq 0$ and $i_A > 0$ in phase-A, the faulty bridge-H_1 and possible faulty switch is either S_{a11} or S_{a14}. The faulty switch is identified by checking the voltage across the diagonal switches (Here; S_{a11} and S_{a14} are diagonal switches). If $v\_{Sa14} = 0$ means faulty switch is S_{a12}, otherwise switch S_{a14}.

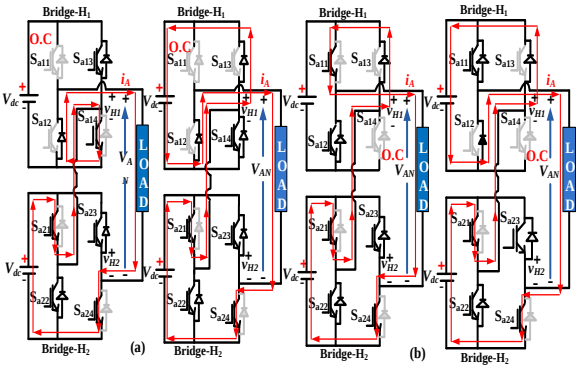

Figure 4. *Case I*; $i_A > 0$, $v_{H1} \leq 0$ fault on bridge-H_1, faulty switches (a) S_{a11}, and (b) S_{a14}.

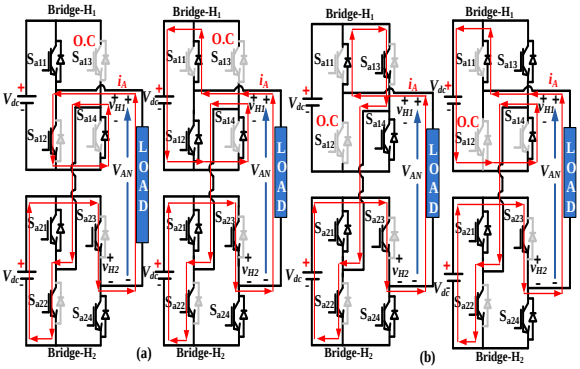

Figure 5. *Case II*; $i_A < 0$, $v_{H1} \geq 0$ fault on bridge-H_1, faulty switches (a) S_{a13}, and (b) S_{a12}.

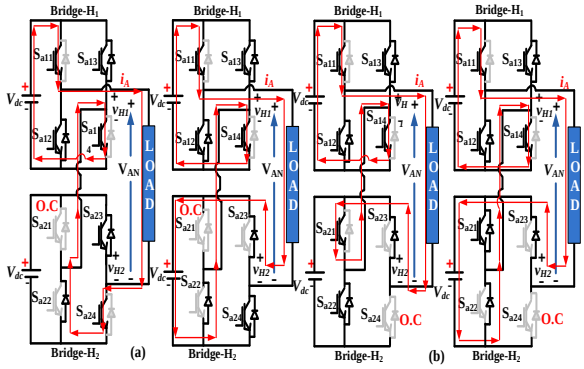

Figure 6. *Case III*; $i_A > 0$, $v_{H2} \leq 0$ fault on bridge-H_2, faulty switches (a) S_{a21}, and (b) S_{a24}

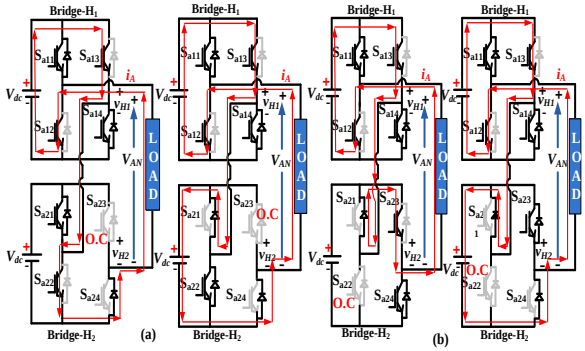

Figure 7. *Case IV*; $i_A < 0$, $v_{H2} \geq 0$ fault on bridge-H_2, faulty switches (a) S_{a23}, and (b) S_{a22}

TABLE 4. Operation and switching sequence during OC fault in switch of 5-level CHBMLI

Sr. No.	Faulty switch/ Circuit diagram	Switching sequence	i_A	v_{H1}	v_{H2}
1	S_{a11} Fig. 4 (a)	S_{a21}, S_{a14}, D_{a12}, S_{a24}	+ve	0	$+V_{dc}$
		S_{a21}, D_{a13}, D_{a12}, S_{a24}	+ve	$-V_{dc}$	$+V_{dc}$
2	S_{a13} Fig. 5 (a)	S_{a23}, S_{a12}, D_{a14}, S_{a22}	-ve	0	$-V_{dc}$
		S_{a23}, D_{a11}, D_{a14}, S_{a22}	-ve	$+V_{dc}$	$-V_{dc}$
3	S_{a14} Fig. 4 (b)	S_{a21}, D_{a13}, S_{a11}, S_{a24}	+ve	0	$+V_{dc}$
		S_{a21}, D_{a13}, D_{a14}, S_{a22}	+ve	$-V_{dc}$	$+V_{dc}$
4	S_{a12} Fig. 5 (b)	S_{a23}, D_{a11}, S_{a13}, S_{a22}	-ve	0	$-V_{dc}$
		S_{a23}, D_{a11}, D_{a14}, S_{a22}	-ve	$+V_{dc}$	$-V_{dc}$
5	S_{a21} Fig. 6 (a)	S_{a11}, S_{a24}, D_{a22}, S_{a14}	+ve	$+V_{dc}$	0
		S_{a11}, D_{a23}, D_{a22}, S_{a14}	+ve	$+V_{dc}$	$-V_{dc}$
6	S_{a23} Fig. 7 (a)	S_{a13}, S_{a22}, D_{a24}, S_{a12}	-ve	$-V_{dc}$	0
		S_{a13}, D_{a21}, D_{a24}, S_{a12}	-ve	$-V_{dc}$	$+V_{dc}$
7	S_{a24} Fig. 6 (b)	S_{a11}, D_{a23}, S_{a21}, S_{a14}	+ve	$+V_{dc}$	0
		S_{a11}, D_{a23}, D_{a22}, S_{a14}	+ve	$+V_{dc}$	$-V_{dc}$
8	S_{a22} Fig. 7 (b)	S_{a13}, D_{a21}, S_{a23}, S_{a12}	-ve	$-V_{dc}$	0
		S_{a13}, D_{a21}, D_{a24}, S_{a12}	-ve	$-V_{dc}$	$+V_{dc}$

3. 2. Faulty Condition For five levels of CHBMLI, each phase consisting two bridges. Under balance condition, there are two isolated neutral points one is the inverter neutral point (P_n) and the other is the load neutral point (N), both of them are at the same potential as shown in Figure 8 (a) and (b). In this figure, all bridges (A_1, A_2, B_1, B_2, C_1, C_2) are healthy, hence the line voltages V_{AB}, V_{BC}, V_{CA} are balanced and form an equilateral triangle with 120^0 phase displacement. When there is a fault at 2nd bridge of phase-A, bridge-A_2 is isolated from the system as shown in Figure 9(a). Hence the line voltages V_{AB}, V_{CA} are disturbed, resulting in unbalance of voltages.

3. 3. Fault Tolerant The simple fault tolerant technique described in literatures are:

(*I*) if there is OC fault at bridge-A_2 of phase-A, bypass or deactivate all its counterparts or same number of bridges from the other healthy phases (i.e., from phase-B, bridge-B_2, and from phase-C, bridge-C_2) to maintain system balanced as shown in Figure 9 (b) [23], so that each phase will have one healthy bridge. However, deactivating the healthy bridge reduce the utilization of the DC-link voltage. This practice is not advisable.

(*II*) Increase the input DC voltage of healthy bridges i.e., if bridge-A_2 has a fault, then increase the voltage of bridge-A_1 to $2V_{dc}$ to compensate the loss of bridge-A_2.

But this leads to increase in voltage stress on the switches. So, increasing the input DC voltage to healthy bridge is also one of the drawbacks. The neutral point shift method is used to overcome these drawbacks, utilizing all the healthy bridges without an increase in voltage stress.

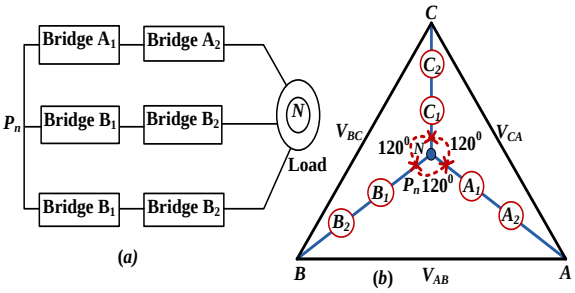

Figure 8. (a) 3-phase, 5-level healthy system (b) line voltages under balanced condition

3. 4. Neutral Point Shift (NPS) Technique The fault-tolerant operation of CHBMLI ensure the continuous operation of the system during and after the fault conditions. The fault-tolerant NPS technique is implemented to balance and maximize the available output line voltages and currents after bypassing the faulty bridge [27]. Normal operating condition, both the neutral points (inverter neutral and load neutral) are at the same potential, and output phase voltages (V_{AN}, V_{BN}, V_{CN}) of CHBMLI are balanced. All phase voltages are displaced by 120^0 and form an equilateral triangle by joining line voltages (V_{AB},V_{BC}, V_{CA}). If OC fault occurs on bridge-H_2 of phase-A, only bridge-H_1 of phase-A contributes to the phase voltage (V_{AN}). This reduces the magnitude of phase voltage which results in unbalanced output line voltages. The magnitude of line voltage V_{AB} and V_{CA} are less than V_{BC}. The phase voltages (V_{AN},V_{BN}, V_{CN}) changes to new phase voltages as L_1, L_2, and L_3 respectively. To maintain the output line voltages and currents balanced, the neutral point of CHBMLI (P_n) is shifted toward a new neutral point (P_n') without disturbing other healthy bridges. The shifting of inverter neutral point (P_n') due to OC fault creates new balanced line voltages 'a'. The new output line voltages form a new equilateral triangle with reduced magnitude than the pre-fault condition. The coordinates (x, y) representation of 3-phase, 5-level CHBMLI with a fault in phase-A of new line voltage 'a' and new phase shift angle (α, β, γ) is shown in Figure 10.

Let (x, y) be the coordinates of new inverter neutral point P_n';

$$L_1^2 = x^2 + y^2 \tag{3}$$

$$L_2^2 = (x-a)^2 + y^2 \tag{4}$$

$$L_3^2 = (x-\tfrac{a}{2})^2 + (y-\tfrac{\sqrt{3}}{2}a)^2 \tag{5}$$

Putting the Equations (4) and (5) in Equation (3), then the new line voltage 'a' is obtained as:

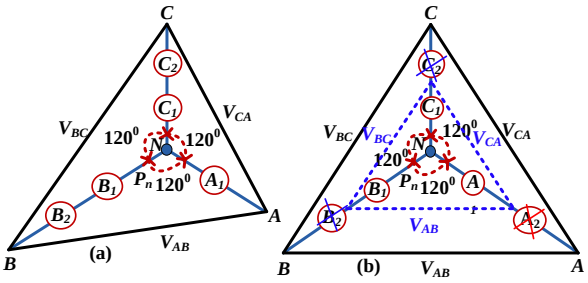

Figure 9. (a) line voltages when OC fault on bridge- A_2 i.e., (1-2-2) (b) Balanced line voltages after bypassing bridges

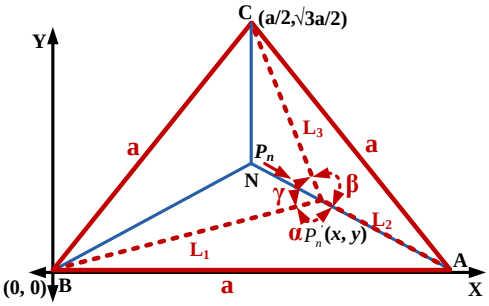

Figure 10. Coordinates representation for parameters calculations

$$a = \sqrt{{L_x}^2 \pm \sqrt{{L_y}^2}} \quad (6)$$

Here, $L_x = \frac{1}{2}\{({L_1}^2 + {L_2}^2 + {L_3}^2)\}$

and $L_y = (6{L_1}^2{L_2}^2 + 6{L_2}^2{L_3}^2 + 6{L_1}^2{L_3}^2 - 3{L_1}^4 - 3{L_2}^4 - 3{L_3}^4)$

$$L_y \geq 0 \quad (7)$$

To meet the Equations (3)-(7), the following condition must be satisfied:

$$L_1 \leq (L_2 + L_3)$$
$$L_2 \leq (L_1 + L_3) \quad (8)$$
$$L_3 \leq (L_2 + L_1)$$

After the calculation of new line voltage 'a', new phase angles are calculated as:

$$\alpha = \cos^{-1}\left(\frac{{L_1}^2 + {L_2}^2 - a^2}{2L_1L_2}\right) \quad (9)$$

$$\beta = \cos^{-1}\left(\frac{{L_2}^2 + {L_3}^2 - a^2}{2L_2L_3}\right)$$

$$\gamma = (360° - \alpha - \beta)$$

From Equation (6), the value of new voltage 'a' depends on L_x and L_y , + sign gives maximum of 'a' and - sign give minimum value of 'a'. After the detection of a fault, the bridge is bypassed and the modulating signal with all three phase angles given by Equation 9 is generated in a controller, and PWM is implemented. The schematic block diagram of the proposed algorithm for fault detection and fault-tolerant along with LSPWM control for the IGBT switch is shown in Figure 11. It consists of D.C source, 3-phase, 5-level CHBMLI, controller, and load. The controller consists of a fault detection technique to detect the fault, and the NPS technique is implemented to control the modulating signal for fault-tolerant, and reassign the modulating signal (i.e.,V_{Aref}, V_{Bref}, V_{Cref}). The generated modulating signals are compared with the multicarrier triangular signal (i.e., LSPWM) and gate pulses are generated to operate MLI.

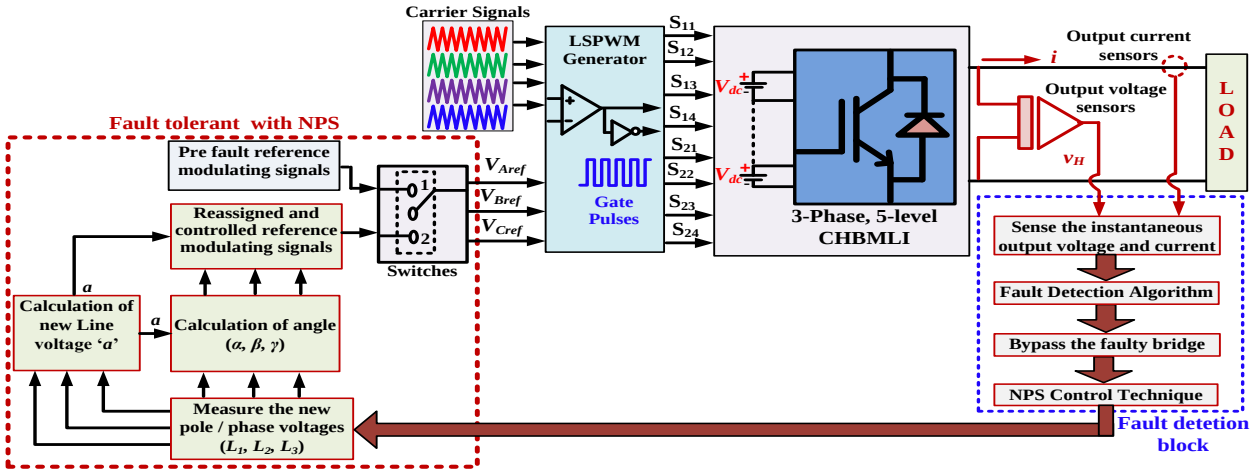

Figure 11. Block diagram of proposed control scheme for 3-phase, 5-level CHBMLI

4. RESULTS AND DISCUSSION

The parameters used for simulation of 3-phase, 5-level CHBMLI with a star-connected RL-load is shown in Table 4. The results are verified with real-time Opal-RT simulator. The LSPWM technique is used for the generation of gate pulses for CHBMLI.

The fault detection algorithm is implemented to detect the OC fault. The operation of the proposed method for fault detection and tolerance is studied for all the cases where as; results for case III and case IV with bridge-H_2 are presented here. In these cases, the fault detection technique senses the instantaneous phase current, instantaneous bridge voltage and instantaneous

TABLE 4. Simulation parameters

Parameters	Ratings
Input DC supply (V_{dc1}=V_{dc2}=V_{dc})	165 V
Load Resistance (R)	10 Ω
Load Inductance (L)	15 mH
Modulation-index (m_a)	1
Modulating signal frequency (f_m)	50 Hz
Carrier signals frequency (f_{cr})	1.5 kHz
PWM technique	LSPWM
Switches	IGBT
Output line voltage	400 V

voltage across switches. Based on the condition corresponding to faulty switch is identified and bypassed for secure and reliable operations. This method detects and tolerates the faulty switch of any phase of the system and, maintains the line voltage and current in balanced condition with the desired magnitude. In case III, an OC fault is created on switch S_{a21} in bridge-H_2 of phase-A, at 0.041s, where the output phase voltage (V_{AN}) and bridge-H_1 output voltage (v_{H1}) are shown in Figure 12 (a) and (b) respectively. The output voltage of bridge-H_2 (v_{H2}) is healthy up to 0.041s which; either becomes 0 or -V_{dc} during fault condition as seen in Figure 12 (c). The change in phase current (i_A) during normal to the faulty condition is observed in Figure 12 (d). The voltage across switch S_{a24} (v_{Sa24}), gate pulse signal for S_{a21}, and the fault detection signal are shown in Figure 12 (e), (f), and (g) respectively.

The fault detection signal goes high at 0.042s thus; the fault which was created at 0.041s is detected at 0.042s. This shows that, in this case the fault detection time is 1 msec. Similarly, in case IV, an OC fault is created on S_{a23} in bridge-H_2 of phase-A at 0.041s, where the output phase voltage (V_{AN}) and bridge-H_1 output voltage (v_{H1}) are plotted in Figure 13 (a) and (b) respectively. Due to fault on S_{a23}, the bridge-H_2 output voltage (v_{H2}) is either 0 or +V_{dc} as shown in Figure 13 (c). The change in current (i_A) during OC fault and voltage across switch (v_{Sa22}) are also shown in Figure 13 (d) and (e) respectively. The gate pulse signal for S_{a23} and the fault detection signal are shown in Figure 13 (f), and (g), respectively.

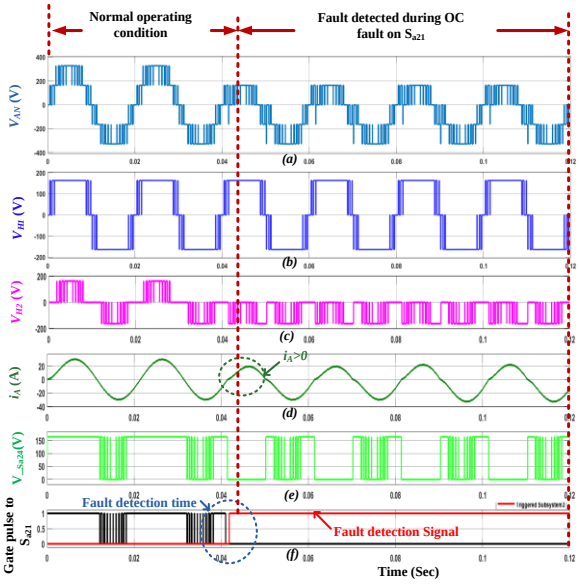

Figure 12. An OC fault on S_{a23}, at t = 0.041 sec (a) output voltage (V_{AN}) (b) Bridge-H_1 output voltage (v_{H1}) (c) Bridge-H_2 output voltage (v_{H2}) (d) output current (i_A) (e) v_{Sa22} signal (f) PWM signal for S_{a23} and (g) fault detection signal (red)

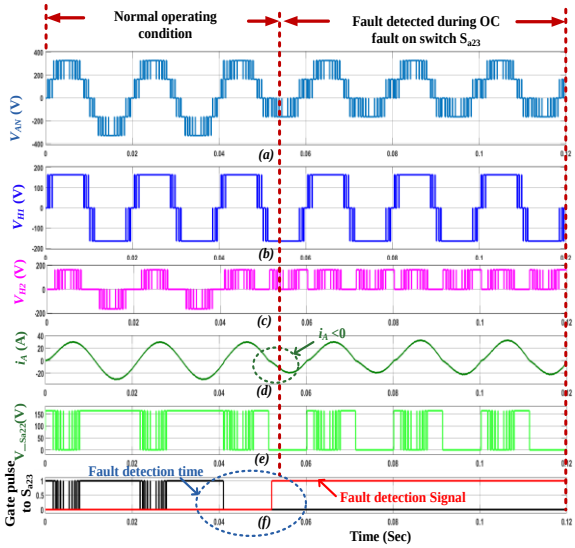

Figure 13. An OC fault on S_{a21} at t = 0.041 sec (a) output line voltage (b) output line current (c) phase-A output voltage (d) Bridge-H_2 output voltage (e) phase-A current (f) PWM signal for S_{a23} (black) and fault detection signal (red)

The fault created at 0.041 s is detected at 0.052 s. Hereby; it shows that, in this case the fault detection time is 11 msec. This time is lowest as compare to other fault detection technique. Hence, the proposed algorithm is validated by the results obtained from MATLAB/Simulink.

In Figures 14, and 15 performances of the proposed fault detection inherent fault isolation capability and fault tolerant by NPS technique is presented. Hence; the waveforms under healthy condition, during fault, and after NPS implementation are studied and analyzed. The 3-phase output line voltages and current waveforms during OC fault, on S_{a21} and their post fault conditions are shown in Figure 14. Similarly, the 3-phase output line voltages and current waveforms during OC fault, on S_{a23} and their post fault conditions are shown in Figure 15. The spectrum analysis of line voltage during various condition like; normal operation, during OC fault, and post fault with NPS implementation without for 3-phase, 5-level CHBMLI configuration.

During normal operating condition, the rms value of the line voltages and the THD is 400 V, 17% respectively as shown in Figure 16. But, during OC fault, the observed rms values of voltage and percentage of THD are different. The rms values of line voltage (V_{AB}) is 326 V and THD is 22%, for V_{BC} it is 400 V and THD is 17%, and for V_{CA} it is 326 V and THD is 23%, as shown in Figure 17. During post fault and after implementation of NPS, the line voltages and currents are balanced with rms value of 343 V and THD = 20%, as shown in Figure 18.

Thus, the results obtained from simulation validates performance of proposed technique for fault detection, inherent isolation capability, and fault tolerant operation.

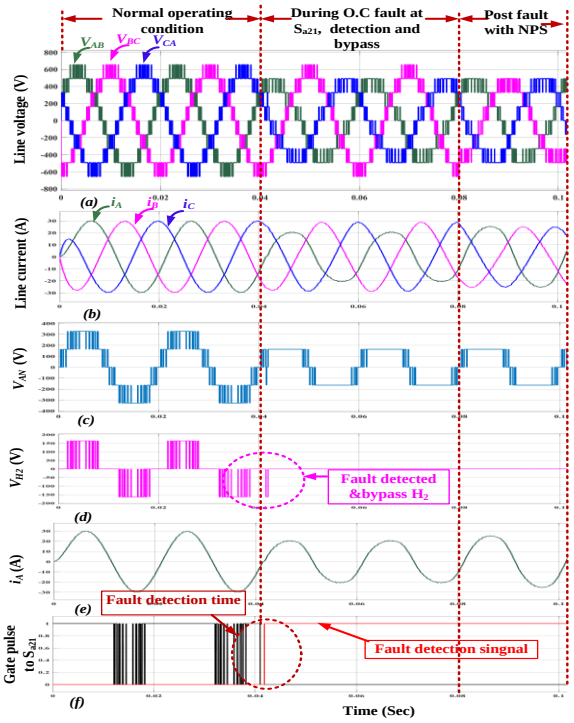

Figure 14. An OC fault on S_{a21} at t = 0.041 sec (a) output line voltage (b) output line current (c) phase-A output voltage (d) Bridge-H_2 output voltage (e) phase-A current (f) PWM signal or S_{a23} (black) and fault detection signal (red)

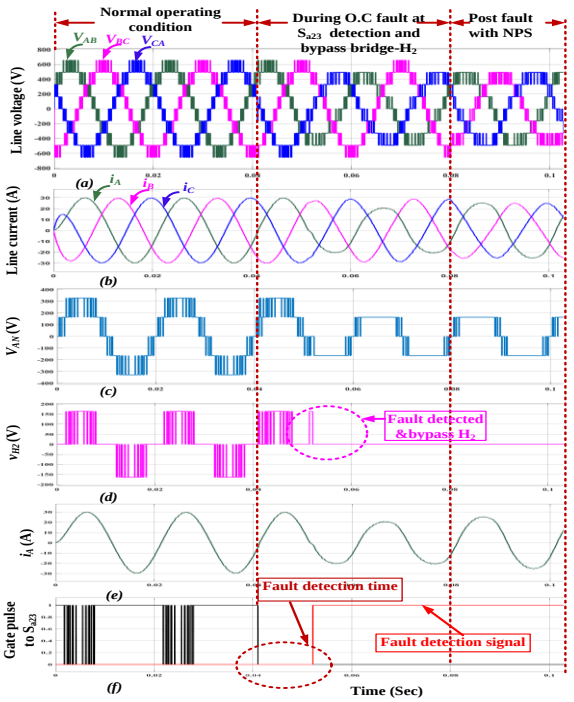

Figure 15. An OC fault on S_{a23} at t = 0.041 sec (a) output line voltage (b) output line current (c) phase-A output voltage (d) Bridge-H_2 output voltage (e) phase-A current (f) PWM signal to S_{a23} (black) fault detection signal (red)

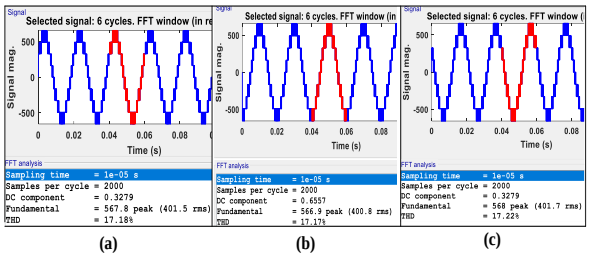

Figure 16. Spectrum analysis of line voltage during Normal operation (a) V_{AB} (b) V_{BC} and (c) V_{CA}

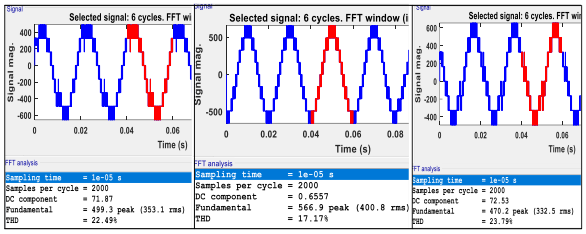

Figure 17. Spectrum analysis of line voltage during OC fault on S_{a23} (a) V_{AB} (b) V_{BC} and (c) V_{CA}

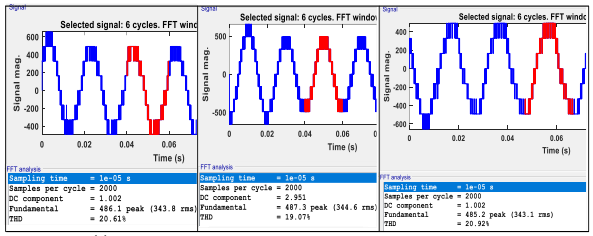

Figure 18. Spectrum analysis of line voltage during post fault with NPS (a) V_{AB} (b) V_{BC} and (c) V_{CA}.

5. OPAL-RT SIMULATOR AND REAL TIME RESULTS

The OP4510 is a family of the latest version of the Opal -RT. It is a firmly united entry-level simulator that consolidates with 128 very fast I/O channels.The OP4510 includes multi-rate FPGA (Kintex-7) with INTEL CPU. The architecture of OP4510 is shown in Figure 19 [28].

An experimental setup of Opal-RT simulator is implemented to examine the proposed algorithm. The proposed algorithm for fault detection, isolation, and fault tolerance is implemented in Simulink and validated in real-time Opal-RT (OP4510) environment. The Opal-RT simulator setup is shown in Figure 20. The simulation is communicated with the Opal-RT real-time simulator via Ethernet cable.

The Opal-RT simulator result of line voltage, line current, phase current (i_A), and phase voltage (V_{AN}) of 3-phase, 5-level CHBMLI under normal operating

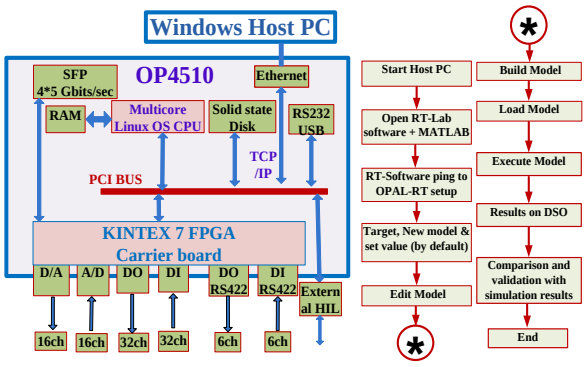

Figure 19. Opal-RT architecture.

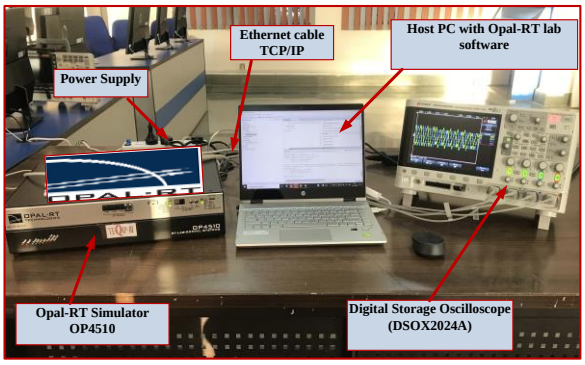

Figure 20. Opal-RT simulator setup

condition can be observed from waveforms shown in Figure 21. In Opal-RT, case III and case IV are studied. In case III, OC fault is created on switch S_{a21} in bridge-H_2 of phase-A. The output voltage of bridge-H_2 (v_{H2}) are $+V_{dc}$, 0, and $-V_{dc}$ which either becomes 0 or $-V_{dc}$ during fault condition, as shown in Figure 22 (a). The v_{Sa21} and change in phase-A current (i_A) during OC fault areshown in Figure 22 (b) and (c) respectively. The gate pulse for S_{a23} and the fault detection signal are shown in Figure 22 (d). Thus, the performance of the developed algorithm is also verified in Opal-RT.

Similarly, for case IV, the proposed technique; under OC fault condition on switch S_{a23} in bridge-H_2 of phase-A is tested in Opal-RT. Where, the bridge-H_1 output voltage (v_{H1}) is not affected entirely as shown in Figure 23 (a). The output bridge-H_2 voltage (v_{H2}) is either 0 or $+V_{dc}$ during OC fault as shown in Figure 23 (b). The phase current (i_A) is deviated during fault condition as shown in Figure 23 (c). The voltage across switch S_{a22} (i.e., v_{Sa22}), gate pulse to S_{a23}, and the fault detection signal are shown in Figure 23 (d), (e), and (f), respectively. The results obtained from MATLAB/Simulink are validated by a real-time simulator for case IV, which detected the faulty switch on bridge-H_2 of phase-A. Figure 24, show the real-time Opal-RT simulator results of the line voltage and line current under pre-fault, during OC fault, and post-fault

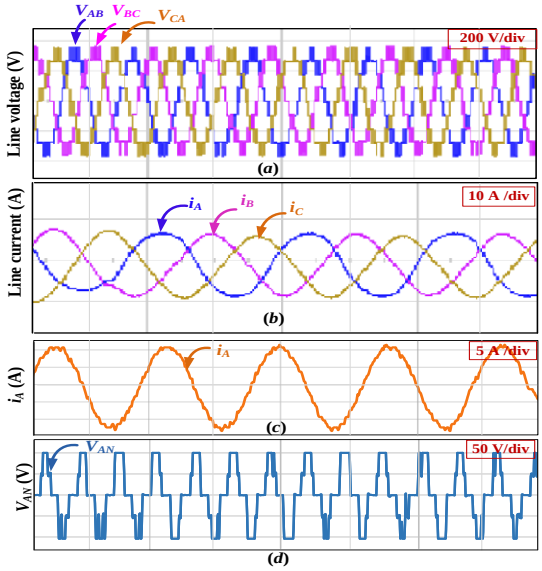

Figure 21. Normal operating condition (a) output line voltage (b) output line current (c) phase current (i_A) (d) phase-A voltage (V_{AN})

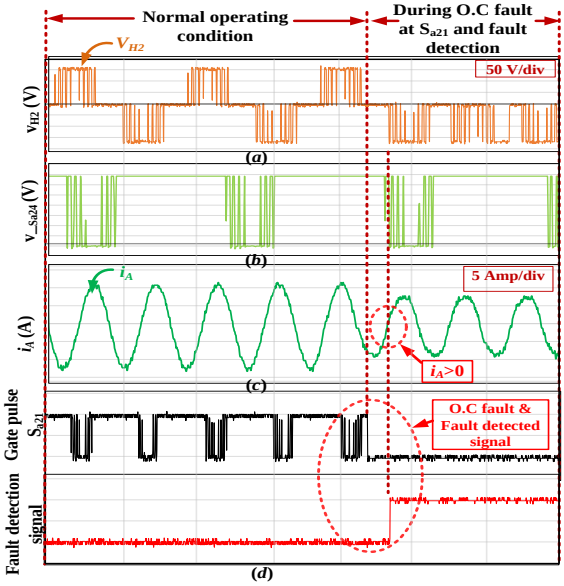

Figure 22. An OC fault on S_{a21} (a) v_{H2} (b) V_{Sa24} (c) i_A (d) gate pulse to S_{a21} and fault detection signal

with NPS technique. The effectiveness of the proposed fault detection algorithm and NPS technique for tolerance under different conditions are evaluated and validated. The comparison of the proposed algorithm with the various existing techniques based on the different features is shown in Table 6. This comparison shows that the proposed algorithm has least fault detection time and provides fault-tolerant operation also. Thus, this algorithm is useful in supplying uninterrupted power to critical loads.

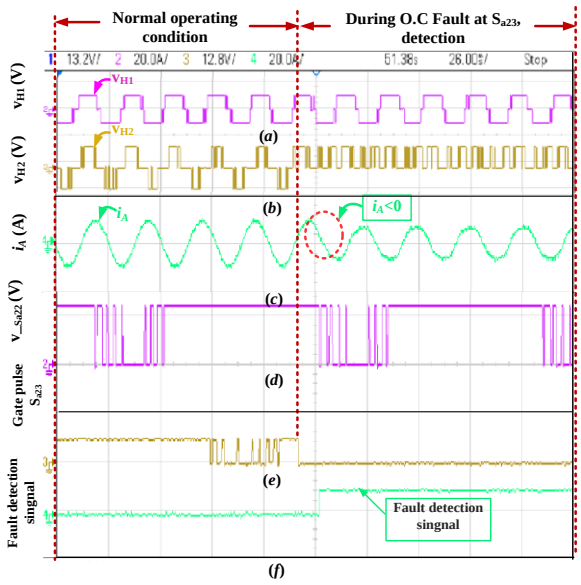

Figure 23. An OC fault on S_{a23} (a) v_{H1} (b) v_{H2} (c) $v_{\_Sa22}$ signal (d) i_A (e) gate pulse to S_{a23} (f) fault detection signal

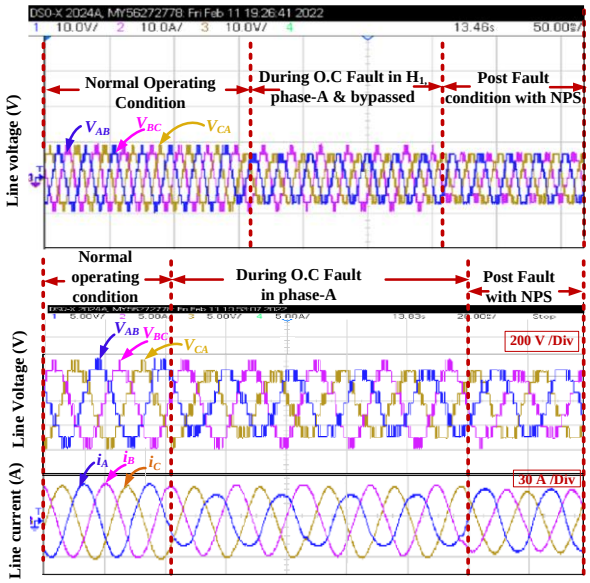

Figure 24. Output line voltage and current under normal operation, during OC fault and post fault with NPS

TABLE 6. Comparison of the proposed technique with the existing technique

Sr. No.	Fault detection methods	Features	Fault detection time	References
1	Based on output current waveform and zero voltage switching states	Fault detection with LSPWM	> 40 msec.	[15]
2	Based on FFT analysis of current signal.	Detect the fault and localize the faulty cells	= 100 msec.	[19]
3	Based on Change in load current during modulating period.	Fault detection and diagnosis	> 60 msec	[20]
4	Based on output voltage and high switching frequency analysis.	• Fault detection • Rejection to normal operation transient	> 30 msec.	[21]
5	Based on Gravitational search algorithm.	Fault detection and fault isolation.	> 30 msec.	[22]
6	Proposed method with instantaneous voltage, current and voltage across switch.	• Fault detection and inherent isolation capability • NPS to fault tolerance • Reliable operation of the system	< 15 msec.	Proposed algorithm

6. CONCLUSION

In this work, a scheme to improve fault detection in 3-phase 5-level CHBMLI is proposed. Table 6, the incorporation of the NPS technique with the proposed algorithm shows a better performance. The OC fault has been detected within minimum reaction time i.e., 15 millisecond. Another advantage of the proposed scheme accompanied by NPS technique is to reschedule the line voltage and current values close to their preferred level. Despite bypassing the faulty bridge, the output line voltages and currents are balanced due to NPS faulttolerant technique during a post-fault condition. The effectiveness of the proposed technique with different cases is validated in MATLAB/ Simulink as well as Opal-RT (OP4510) simulator. The results obtained by Opal-RT simulator confirm the fast detection, isolation of faulty bridges, and fault tolerance. Thus, the developed algorithm is useful in supplying uninterrupted power to critical loads.

7. REFERENCES

1. Rodríguez, J., Bernet, S., Wu, B., Pontt, J.O. and Kouro, S., "Multilevel voltage-source-converter topologies for industrial medium-voltage drives", ***IEEE Transactions on Industrial Electronics***, Vol. 54, No. 6, (2007), 2930-2945. doi: 10.1109/TIE.2007.907044.
2. Rahimi Mirazizi, H. and Agha Shafiyi, M., "Evaluating technical requirements to achieve maximum power point in photovoltaic powered z-source inverter", ***International Journal of Engineering, Transactions C: Aspects***, Vol. 31, No. 6, (2018), 921-931. doi: 10.5829/IJE.2018.31.06C.09.

3. Alemi-Rostami, M. and Rezazadeh, G., "Selective harmonic elimination of a multilevel voltage source inverter using whale optimization algorithm", ***International Journal of Engineering, Transactions B: Applications***, Vol. 34, No. 8, (2021), 1898-1904. doi: 10.5829/IJE.2021.34.08B.11.
4. Saketi, S.K., Chaturvedi, P., Yadeo, D. and Atkar, D., "A reliable and efficient modified t-type fault tolerant five level inverter configuration", ***International Transactions on Electrical Energy Systems***, Vol. 31, No. 8, (2021), e12975. doi: 10.1002/2050-7038.12975.
5. Sabyasachi, S., Borghate, V.B., Karasani, R.R., Maddugari, S.K. and Suryawanshi, H.M., "Hybrid control technique-based three-phase cascaded multilevel inverter topology", ***IEEE Access***, Vol. 5, (2017), 26912-26921. doi: 10.1109/ACCESS.2017.2727551.
6. Arehpanahi, M. and Paknia, D., "A new single-phase symmetrical cascade multilevel inverter with low number of power switches", ***International Journal of Engineering, Transactions B: Applications***, Vol. 31, No. 8, (2018), 1228-1233. doi: 10.5829/ije.2018.31.08b.10.
7. Tousi, B. and Ghanbari, T., "Transformer-based single-source multilevel inverter with reduction in number of transformers", ***International Journal of Engineering, Transactions B: Applications***, Vol. 29, No. 5, (2016), 621-629. doi: 10.5829/idosi.ije.2016.29.05b.05.
8. Poorfakhraei, A., Narimani, M. and Emadi, A., "A review of multilevel inverter topologies in electric vehicles: Current status and future trends", ***IEEE Open Journal of Power Electronics***, Vol. 2, (2021), 155-170. doi: 10.1109/ OJPEL.2021.3063550.
9. Vemuganti, H.P., Sreenivasarao, D., Ganjikunta, S.K., Suryawanshi, H.M. and Abu-Rub, H., "A survey on reduced switch count multilevel inverters", ***IEEE Open Journal of the Industrial Electronics Society***, Vol. 2, (2021), 80-111. doi: 10.1109/OJIES.2021.3050214.
10. Maharjan, L., Yamagishi, T., Akagi, H. and Asakura, J., "Fault-tolerant operation of a battery-energy-storage system based on a multilevel cascade pwm converter with star configuration", ***IEEE Transactions on Power Electronics***, Vol. 25, No. 9, (2010), 2386-2396. doi: 10.1109/TPEL.2010.2047407.
11. Malinowski, M., Gopakumar, K., Rodriguez, J. and Perez, M.A., "A survey on cascaded multilevel inverters", ***IEEE Transactions on Industrial Electronics***, Vol. 57, No. 7, (2009), 2197-2206. doi: 10.1109/TIE.2009.2030767.
12. Valipour, S., Moosavi, S.S., Khaburi, D.A. and Djerdir, A., "An open-circuit fault detection method using wavelet transform for cascaded h-bridge multilevel inverter", in 2017 IEEE Vehicle Power and Propulsion Conference (VPPC), IEEE. (2017), 1-5.
13. Zhang, G. and Yu, J., "Open-circuit fault diagnosis for cascaded h-bridge multilevel inverter based on ls-pwm technique", ***CPSS Transactions on Power Electronics and Applications***, Vol. 6, No. 3, (2021), 201-208. doi: 10.24295/ CPSSTPEA.2021.00018.
14. Choi, U.-M., Blaabjerg, F. and Lee, K.-B., "Study and handling methods of power igbt module failures in power electronic converter systems", ***IEEE Transactions on Power Electronics***, Vol. 30, No. 5, (2014), 2517-2533. doi: 10.1109/TPEL.2014.2373390.
15. Sim, H.-W., Lee, J.-S. and Lee, K.-B., "A detection method for an open-switch fault in cascaded h-bridge multilevel inverters", in 2014 IEEE Energy Conversion Congress and Exposition (ECCE), IEEE. (2014), 2101-2106.
16. Faraz, G., Majid, A., Khan, B., Saleem, J. and Rehman, N., "An integral sliding mode observer based fault diagnosis approach for modular multilevel converter", in 2019 International Conference on Electrical, Communication, and Computer Engineering (ICECCE), IEEE. (2019), 1-6.
17. Anand, A., Akhil, V.B., Raj, N., Jagadanand, G. and George, S., "An open switch fault detection strategy using mean voltage prediction for cascaded h-bridge multilevel inverters", in 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), IEEE. (2018), 1-5.
18. He, J., Demerdash, N.A., Weise, N. and Katebi, R., "A fast on-line diagnostic method for open-circuit switch faults in sic-mosfet-based t-type multilevel inverters", ***IEEE Transactions on Industry Applications***, Vol. 53, No. 3, (2017), 2948-2958. doi: 10.1109/TIA.2016.2647720.
19. Thantirige, K., Rathore, A.K., Panda, S.K., Mukherjee, S., Zagrodnik, M.A. and Gupta, A.K., "An open-switch fault detection method for cascaded h-bridge multilevel inverter fed industrial drives", in IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society, IEEE. (2016), 2159-2165.
20. Zhang, J., Empringham, L., De Lillo, L., Dan, H. and Wheeler, P., "Matrix converter open circuit fault diagnosis with asymmetric one zero svm", in 2017 IEEE Energy Conversion Congress and Exposition (ECCE), IEEE. (2017), 3470-3475.
21. Lezana, P., Aguilera, R. and Rodríguez, J., "Fault detection on multicell converter based on output voltage frequency analysis", ***IEEE Transactions on Industrial Electronics***, Vol. 56, No. 6, (2009), 2275-2283. doi: 10.1109/IECON.2006.347999.
22. Vyas, U.B., Shah, V.A. and SG, S., "Fault detection technique for modified cascaded half-bridge multi-level inverter with polarity changer in pv grid system", ***SN Applied Sciences***, Vol. 3, No. 5, (2021), 589. https://doi.org/10.1007/s42452-021-04586-5
23. Deepak, A. and Das, A., "Operation of cascaded h-bridge converter with bypassed cells during fault conditions", in 2016 IEEE International Conference on Industrial Technology (ICIT), IEEE. (2016), 1220-1225.
24. Eaton, D., Rama, J. and Hammond, P., "Neutral shift [five years of continuous operation with adjustable frequency drives]", ***IEEE Industry Applications Magazine***, Vol. 9, No. 6, (2003), 40-49. doi: 10.1109/MIA.2003.1245795.
25. Kumar, R., Chaudhari, M.A., Chaturvedi, P. and Sekhar, K.R., "Dynamic operation of ac micro-grid integrated pv-bess using 3-phase97-level chbmli", in 2022 International Conference on Green Energy, Computing and Sustainable Technology (GECOST), IEEE. (2022), 11-17.
26. Wu, B. and Narimani, M., "High-power converters and ac drives, John Wiley & Sons, (2017).
27. Khaire, N.C., Chaudhari, M.A. and Kumar, R., "Fault-tolerant operation of 3-phase 7-level chbmli with modified neutral point shift method", in 2022 Second International Conference on Power, Control and Computing Technologies (ICPC2T), IEEE. (2022), 1-6.
28. Rajkumar, K., Parthiban, P. and Lokesh, N., "Real-time implementation of transformerless dynamic voltage restorer based on t-type multilevel inverter with reduced switch count", ***International Transactions on Electrical Energy Systems***, Vol. 30, No. 4, (2020), e12301. https://doi.org/10.1002/2050-7038.12301

Persian Abstract

چکیده

تشخیص عیب و بازیابی آن چالش اصلی برای عملکرد روان اینورتر چند سطحی (MLI) است. در این مقاله، تشخیص عیب و طرح پاکسازی آن برای یک خطای مدار باز (OC)در یک اینورتر چند سطحی پل H آبشاری ۳ سطحی ۵ سطحی (CHBMLI)توسعه و آزمایش شده است تا قابلیت اطمینان و مناسب بودن را بهبود بخشد. سیستم. تشخیص دقیق و سریع، جداسازی و دور زدن پل‌های معیوب، قابلیت اطمینان، تناسب و مقبولیت CHBMLI را در هر کاربرد خانگی و صنعتی درایو افزایش می‌دهد. برای تغییر زمان ولتاژ خط و مقدار جریان نزدیک به سطح پیش از خطا، یک تکنیک تغییر نقطه خنثی (NPS) در این مقاله ارائه شده است. ولتاژ خروجی مورد نظر توسط تکنیک Level Shift Pulse Width Modulation (LSPWM) کنترل می شود. طرح پیشنهادی در محیط MATLAB/Simulink توسعه یافته و نتایج با استفاده از شبیه‌ساز Opal-RT تایید می‌شوند. نتایج شبیه‌سازی عملکرد را تأیید کرده است و نتایج شبیه‌ساز Opal-RT امکان‌سنجی و کاربردی بودن طرح پیشنهادی را نشان می‌دهد.