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Taguchi Approach and Response Surface Analysis for Design of a High-performance Single-walled Carbon Nanotube Bundle Interconnects in a Full Adder

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ABSTRACT

In this study, it was attempted to design a high-performance single-walled carbon nanotube (SWCNT) bundle interconnects in a full adder. For this purpose, the circuit performance was investigated using simulation in HSPICE software and considering the technology of 32-nm. Next, the effects of geometric parameters including the diameter of a nanotube, distance between nanotubes in a bundle, and width and length of the bundle were analyzed on the performance of SWCNT bundle interconnects in a full adder using Taguchi approach (TA). The results of Taguchi sensitivity analysis (TSA) showed that the bundle length is the most effective parameter on the circuit performance (about 51% on the power dissipation and 47% on the propagation delay). Moreover, the distance between nanotubes greatly affects the response compared to other parameters. Also, response surface method (RSM) indicated that an increase in the length of interconnects (L) improves the output of power dissipation. As the width of interconnects (W) and diameter of CNTs (D) increase the power dissipation also increases. Decrease in the distance between CNTs in a bundle (d) leads to an increase in power dissipation. The highest value of power dissipation is achieved if the maximum values for the parameters of length and width of interconnects (L, W), and diameter of CNTs (D) and the minimum value of the distance between CNTs in a bundle (d) are considered. It is also revealed that an increase in the length of interconnects (L) increases the propagation delay. Eventually, the optimum parameters are reported and the performance of the optimized system is compared using different methods (TA and RSM). Results indicate that the difference between the performance of optimal design of SWCNT bundle interconnects in a full adder predicted by different methods is less than 6% which is acceptable according to engineering standards.

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1. INTRODUCTION

As the design and fabrication of highly compact integrated circuits are developing, efforts to shrink the on-chip feature sizes down to 30 nm and below continue. However, for interconnect materials based on copper (Cu), such reduction in fabrication sizes adversely affects the performance (increase in propagation delay through interconnect) and reliability because of an increased resistance and current density [1]. Application of the traditional interconnects based on Cu in the nanometer region is limited due to the low thermal and electrical conductivity [2], short mean free path [3], high resistivity [4], and electro-migration [5]. Therefore, innovative technological solutions and alternative material combinations are required for the interconnect applications, which exceed the performance of Cu and are superior to Cu in reliability. So far, various technologies presented by researchers are based on Carbon Nanotube Field Effect Transistor (CNTFET), Single Electron Transistors (SET), Quantum-Dot Cellular Automata (QCA), and Multi Gate Field Effect Transistor (MUGFET) [6–9].

CNT bundles are specific scientific interest and are an appropriate choice for replacing copper interconnects because of their intrinsic characteristics such as high

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resistance, electrical, thermal, magnetic, and mechanical properties. The van der Waals forces form stabilized bundles of CNTs [10]. Current density of CNT is 1011 A/cm^2 or more, which is higher than that of Cu (depending on the fabrication process and used capping layer is in the range of 106-107 A/cm^2) [11]. Therefore, due to the high carrying current densities of CNT, damage could be prevented where the highest current densities are expected, even at high temperatures [12]. Additionally, Srivastava and Banerjee [13] have reported that the minimum value of interconnect propagation delay occurs at the optimum density. This optimal density is always less than the maximum packing density of CNT bundles. Also, it has been stated in previous research that the thermal conductivity and tensile strength of CNTs are respectively three and two times larger than those of Cu wires [14]. Moreover, due to the weak influence of the CNT's length of resistance, the distance between the interconnect levels can be increased [11].

A CNT bundle interconnect can consist of single-walled carbon nanotubes (SWCNT) or multi-walled carbon nanotubes (MWCNT). In MWCNTs, achieving ballistic transport over long lengths is problematic, however the MWCNTs are metallic [13]. A SWCNT uses a single graphene sheet rolled up into a cylindrical tube with a variable diameter (0.4 to 4 nm). Depending on the chirality vector, the SWCNT could be either metallic or semi-conducting [15]. In general, semi-conductive nanotubes are applied for the channel of carbon nanotube field-effect transistors (CNFETs) [5]. It is noteworthy that the average electron free paths of SWCNT are about one micron [16]. According to the result obtained by Rai and Sarkar [12], the power dissipation increases as CNT's diameter increases and capacitance in SWCNT interconnect decreases. Thus, in the manufacturing process of SWCNT samples, technologists cope with the challenges in controlling the SWCNT's length, diameter, width, and the preparation due to control of equivalent circuit impedance parameters [17].

Resistances and capacitances are the main effective factors on the stability and the time domain responses of an inductance interconnect [18]. Some research efforts have addressed the different stability prospects of CNTs. In this regard, Xu et al. [19] have reported the mechanical and thermal stability of CNTs. They claimed that a zigzag CNT has a better stability than that of an armchair CNT with the same diameter. Chiodarelli et al. [11] focused on the optical stability of CNTs. Fathi and Forouzandeh [3] presented the Nyquist stability diagrams of CNTs interconnects. The authors offered a new concept for CNT interconnects named as "relative stability". They stated that the relative stability of the CNT bundle increases as the diameter and the length of the CNT bundle increase. Moreover, Zhao et al. [10] demonstrated that the technology advancement may lead to increased damping property and suppress the fluctuation in the time domain step response. Shin et al. [20] have discussed about the chemical stability of CNTs. They suggested general guidelines for ensuring the stability of CNTs against acid treatments.

CNFET transistors are used to design the full adder cell as one of the essential blocks of the arithmetic circuits because of its high performance and low power consumption properties [21]. It is well known that the full adder plays an important role in ALUs, CPUs, address generation and memory access units since its functionality has a great impact on the whole system's functionality [22]. Several groups have proposed the enhanced performance of full adder circuits in terms of functionality. For instance, Nejadzadeh and Reshadinezhad [22] have improved the performance of CNFET-based full adder regarding time delay and PDP by reducing the transistors count and critical paths and increasing the reliability of the circuit. Zhao et al. [10] have proposed a full adder based on hybrid-CMOS that was implemented by 24 transistors. Also, the new full adder based on CNFETs circuit improved the PDP, power consumption, and performance of the full adder cell [23]. Ghanaghestani et al. [24] have suggested a full adder cell based on a parallel design using CNFETs. The suggested model affects the power consumption and speed, which results in reducing the critical path delay. A CNFET full adder circuit design demonstrated by Ghorbani et al. [25] significantly improved both delay and power outputs, which is able to work in a wide range of temperatures, load capacitors, and frequencies. Sharifi et al. [26], in their approaches, significantly reduced the complexity and energy consumption of the full adder's design by using novel quaternary-to-binary and binary-to-quaternary converters. The validation process of the performance of the proposed model has been done using HSPICE simulator. Torkzadeh Mahani and Keshavarzian [27] have proposed new full adder circuits based on CNTFET and GDI structure, which result in better drive capacity and output swing, less energy consumption, power consumption, delay, EDP, and better parameters in higher frequencies.

Despite all past researches, the simultaneous effects of the geometric parameters of SWCNT bundle interconnects on the power dissipation and propagation delay in a full adder have not been investigated. Therefore, for the first time this was accomplished by applying Design of Experiment (DOE) techniques including Taguchi approach and response surface method. Finally, the geometrical parameters (diameter of a nanotube, distance between nanotubes in a bundle, and width and length of the bundle) were optimized to achieve the best system performance. The obtained results were verified by comparison with the HSPICE simulator.

2. DETAILED DISCUSSIONS REGARDING THE THEORIES OF CURRENT MODELS BY SWCNT BUNDLE IN A FULL ADDER

An equivalent circuit model of an isolated SWCNT interconnect, including various electrical components (e. g., resistance, capacitors, and inductance) is shown in Figure 1, in which, parameters R, L, and C are the resistance, inductance and capacitor, respectively. Also, the indices C, Q, S, M, K, and E represent connection, quantum, diffraction, magnetic, kinetic, and electrostatic, respectively. The single-walled carbon nanotube structure on a ground plane is illustrated in Figure 2, in which, Y is distance between the SWCNT center and the ground plane. The diameter of outermost shell of SWCNT is referred to D. SWCNTs are composed of one shell of carbon atoms. SWCNTs adhere strongly to each other forming ropes or bundles of nanotubes. The diameter of the most SWCNTs is about one nanometer, and the tube length can be several thousands times longer. The structure of a SWCNT can be achieved by folding an atomic thick layer of graphene into a tubular structure. SWCNT is characterized by its chirality, which determines its properties and diameter. The chirality is represented with a pair of indices (n, m), which is called the chiral vector. The chiral vector traces the CNT around its circumference from one carbon atom back to itself. CNTs are classified into three groups: armchair nanotubes for n = m, zigzag nanotubes for m = 0 or n = 0, and chiral nanotubes for any other combination [28]. The conductive properties of CNTs are determined by its helicity, diameter, and chirality.

Next, a brief description of the theories related to each of the electrical components used in the proposed model (Figure 1) is discussed.

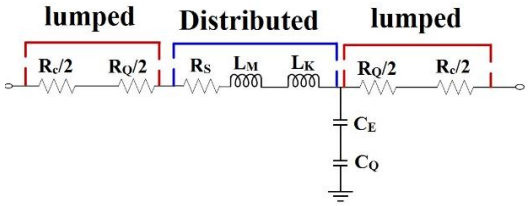

Figure 1. Details of the circuit model of an isolated SWCNT interconnect

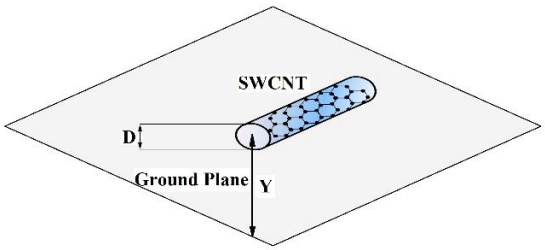

Figure 2. SWCNT structure on a ground plane

2. 1. Resistance of SWCNT The total resistance of a SWCNT (R_{CNT}) is calculated by applying Equation (1). The value of R_C is in the range of 10 Ω to 100 kΩ [29]. Also, the values of quantum resistance (R_Q) and diffraction resistance (R_S) may be obtained as follows:

$$R_{CNT} = \sum R_i = R_C + R_Q + R_S \quad (1)$$

$$R_Q = \frac{h}{4e^2} \quad (2)$$

$$R_S = \begin{cases} R_Q \times \frac{L}{\lambda_{mfp}} & if\ L > \lambda_{mfp} \\ 0 & if\ L < \lambda_{mfp} \end{cases} \quad (3)$$

where e is the electron charge, h is the Planck constant, L is the length of a carbon nanotube, and λ_{mfp} is the mean free distance ($\lambda_{mfp} = 2 \times 10^3 \times r_{CNT}$, and r_{CNT} is the radius of a carbon nanotube) [30].

2. 2. Capacitor of SWCNT The electrostatic capacitor (C_E) and quantum capacitor (C_Q) are defined as:

$$C_E = \frac{2\pi\varepsilon_r\varepsilon_0}{Ln\frac{Y}{D}} \quad (4)$$

$$C_Q = \frac{4e^2}{hV_f} \quad (5)$$

As previously expressed in Figure 2, Y and D are the distance of carbon nanotube's center from ground and diameter of carbon nanotube, respectively. Also, the relative and vacuum dielectric coefficients are called ε_r and ε_0, respectively. Moreover, V_F is Fermi velocity equal to $8 \times 10^5\ m/s$ for graphene and carbon nanotube [31].

2. 3. Inductance of SWCNT The kinetic and magnetic inductances are also calculated by employing Equations (6) and (7). Since the value of L_M is less than that of L_K, it must be ignored [32].

$$L_K = \frac{h}{4e^2V_f} \quad (6)$$

$$L_M = \frac{\mu_0}{2\pi} \times \ln\left(\frac{Y}{D}\right) \quad (7)$$

where μ_0 is the carrier mobility. Figure 3 shows the cross-section of the SWCNT bundle. Also, the total number of nanotubes (N_{CNT}) may be obtained as following:

$$N_{CNT} = \begin{cases} N_X N_Z - \frac{N_Z}{2} & if\ N_Z = even \\ N_X N_Z - \frac{N_Z - 1}{2} & if\ N_Z = odd \end{cases} \quad (8)$$

where N_X and N_Z are the number of nanotubes in directions X and Z, respectively.

$$N_X = \frac{W-D}{X} \quad (9)$$

$$N_Z = \frac{2(t-D)}{\sqrt{3}\,X} + 1 \quad (10)$$

In these equations, W and t are the width and thickness of bundle, D is the diameter of nanotubes, and X is the distance between centers of two adjacent carbon nanotubes. Also, the specifications of interconnects in different lengths and also their drivers in 32-nm technology based on ITRS 2013 are presented in Table 1. Next, values of resistance, capacitor, and inductance of carbon nanotube bundles are calculated based on Equations (11)-(13) [13].

$$R \rightarrow R_{Bundle} = \frac{R_C + R_Q + R_S}{N_{CNT}} \tag{11}$$

$$C \rightarrow \begin{cases} C_Q^{Bundle} = C_Q \times N_{CNT} n \\ C_E^{Bundle} = 2C_{En} + \frac{N_X - 2}{2} \times C_{Ef} + \frac{3(N_Z - 2)}{5} \times C_{En} \\ C_{En} = \frac{2\pi\varepsilon_r\varepsilon_0}{ln\left(\frac{S}{D}\right)} \quad and \quad C_{Ef} = \frac{2\pi\varepsilon_r\varepsilon_0}{ln\left(\frac{S+W}{D}\right)} \\ C_{Bundle} = L \times \frac{C_Q^{Bundle} \times C_E^{Bundle}}{C_Q^{Bundle} + C_E^{Bundle}} \end{cases} \tag{12}$$

$$I \rightarrow \begin{cases} L_m^{Bundle} = L_m \\ L_k^{Bundle} = \frac{L_k}{N_{CNT}} \\ L_{Bundle} = \frac{L \times L_k^{Bundle}}{N_{CNT}} \end{cases} \tag{13}$$

Eventually, the full adder's block diagram used in the present research is depicted in Figure 4. It was simulated in 32-nm technology using HSPICE software. In simulations, the carbon nanotube-based field effect transistors were used. In this scheme, interconnects are shown by red color and short circuit is the ideal state. But these lines can be made up of cooper in new technologies and carbon nanotube bundles in nanoscale.

3. TAGUCHI APPROACH

In this method, according to certain rules, a set of tables is prepared as an orthogonal array. These arrays make it possible to examine the main and interaction effects of different parameters by performing the least number of experiments. In fact, it is the biggest advantage of the Taguchi method over other DOE techniques. Taguchi proposes two models for analyzing results (standard and signal to noise ratio). The standard model works based on the calculating the effect of factors and performing analysis of variance. The second method examines the scattering near a certain amount. As the value of this ratio (signal to noise) increases, the amount of scattering decreases, and in this case the effect of that parameter will be more important.

In the present research, four geometric parameters with three different levels as reported in Table 2, were used to perform Taguchi analysis. To this end, a used general algorithm including the input variables and responses is depicted in Figure 5.

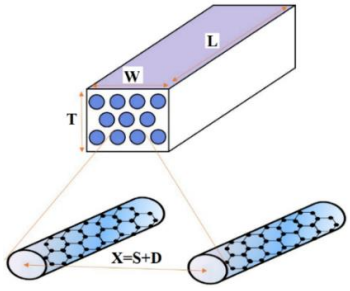

Figure 3. Cross section of a carbon nanotube bundle

TABLE 1. Specifications of interconnects in 32-nm technology

Parameter	Unit	Value	
		Global	Local & intermediate
V_{DD}	V	0.9	0.9
Width (W)	nm	40	32
Thickness (T)	nm	120	64
Aspect ratio (A/R)	-----	3	2
Oxide thickness (t_{OX})	nm	93.6	54.4
Dielectric constant	-----	2.77	2.25
Separation between adjacent bundles	nm	40	32
Center to center SWCNT in bundle (d)	nm	0.34	0.34
Diameter of SWCNT (D)	nm	1	1
ρ_0 for cu	uΩ cm	3.66	4.81
R_t	kΩ	13.85	13.85
C_{out}	fF	0.07	0.07
C_{in}	fF	0.25	0.25

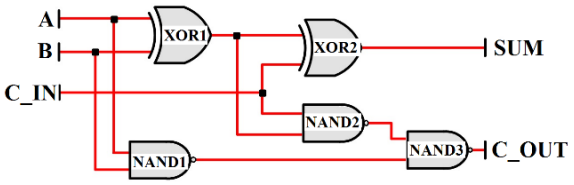

Figure 4. The full adder's block diagram used in this study

TABLE 2. Variables and their levels used as input data in the Taguchi-based DOE

Parameters	Symbol	Levels		
		L1	L2	L3
Length of interconnects	L	10 um	50 um	100um
Width of interconnects	W	30 nm	40 nm	50 nm
Diameter of CNTs	D	1 nm	2 nm	4 nm
Distance between CNTs in a bundle	d	0 nm	0.34 nm	1 nm

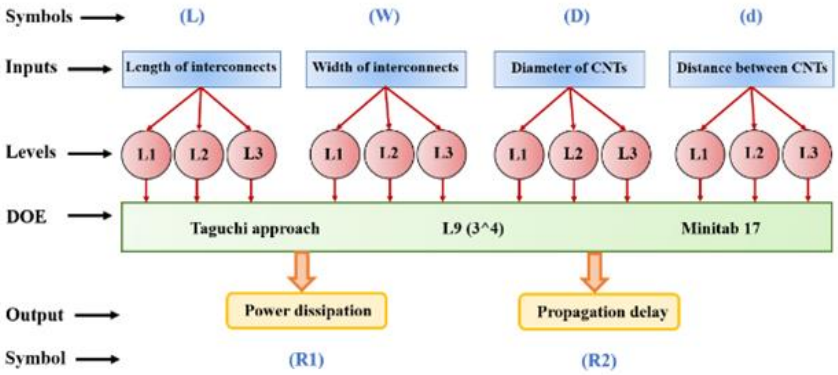

Figure 5. The scheme of Taguchi-based design of experiments used in this study

4. RESPONSE SURFACE ANALYSIS

RSM is a set of measurable systems and applied science to develop test models. The point of such plan is to optimize the output which is influenced by a few factors. Thusly, variations of the factors are made to detect the reasons for changes in the response [33, 34]. To decrease the computational costs (e. g., simulation and solving time), the prediction algorithm of Taguchi was utilized to estimate the desired cases [33].

5. RESULTS AND DISCUSSION

The circuit performance of CNT bundle interconnects in a full adder for the various cases (suggested by DOE) was analyzed using simulation in HSPICE software and considering the technology of 32-nm. The obtained results of simulation are presented in Table 3. In the current research, two outputs including power dissipation and propagation delay were investigated as representing the performance of the system. In general, research seeks to reduce propagation delay or reduce power dissipation in the system, both of which mean an increase in system performance. Therefore, the viewpoint of smaller is better was considered for both responses as follows [35]:

$$S/N = -10Log\left[\frac{1}{n}(y_1^2 + y_2^2 + \cdots + y_n^2)\right] \quad (14)$$

where y_1, y_2 , and y_n are the measured bent angles in the bending process, and each bending condition is repeated n times.

Afterward, the influences of S/N and mean ratios at every level were analyzed and the results are demonstrated in Figures 6 and 7 for power dissipation and propagation delay, respectively. It is clearly obvious from Figures 6 and 7, the number of experiments with 4 factors in three levels is enough to conduct TA. Because, the trend of S/N ratios diagram is completely reverse

TABLE 3. HSPICE simulation results extracted for TA

Experiment No.		Power dissipation (uw)	Propagation delay (ns)
1	L=10 um W=30 nm D=1 nm d=0 nm	1.3285	1.7334
2	L=10 um W=40 nm D=2 nm d=0.34 nm	1.3274	1.7478
3	L=10 um W=50 nm D=4 nm d=1 nm	1.320	1.7310
4	L=50 um W=30 nm D=2 nm d=1 nm	1.4551	1.7436
5	L=50 um W=40 nm D=4 nm d=0 nm	1.7609	1.7535
6	L=50 um W=50 nm D=1 nm d=0.34 nm	1.5224	1.7531
7	L=100 um W=30 nm D=4 nm d=0.34 nm	1.9607	1.7794
8	L=100 um W=40 nm D=1 nm d=1 nm	1.6009	1.7764
9	L=100 um W=50 nm D=2 nm d=0 nm	2.0892	1.7504

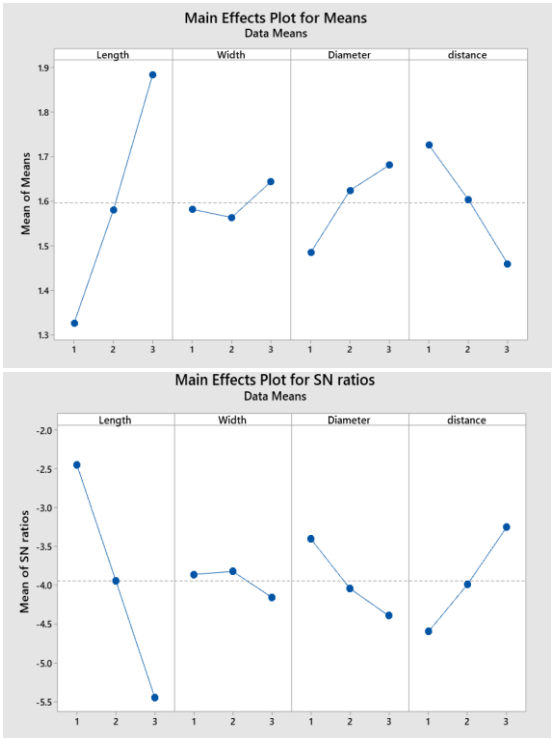

Figure 6. Influences of S/N and mean ratios of all parameters related to power dissipation

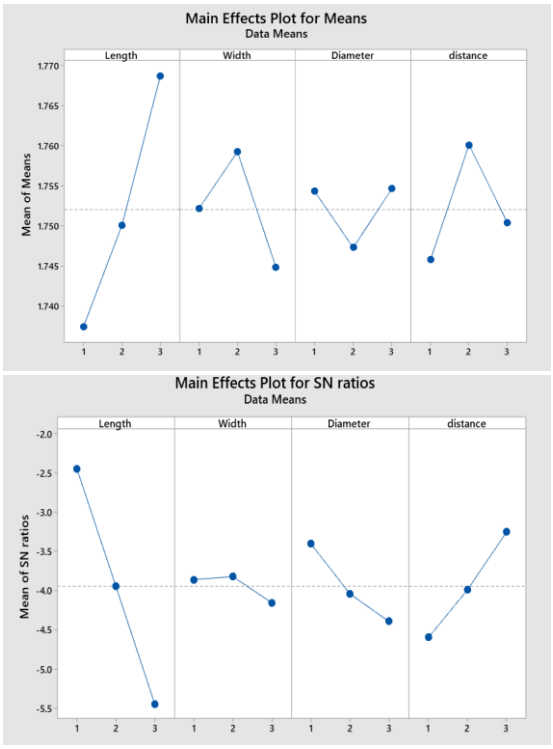

Figure 7. Influences of S/N and mean ratios of all parameters related to propagation delay

compared with trend of mean ratios diagram. As shown in Figure 7, the trend of power dissipation changes in terms of all parameters (L, D, and d) is linear except for the width of the bundle (W). This behavior is also seen at the output of the propagation time. Therefore, the value of this parameter (W) can affect the behavior of the response to other parameters. As a result, it is strongly necessary to examine the behavior of the system in a multi-dimensional way (the interaction effects of parameters).

Also, Figure 8 demonstrates the influence ranking of the geometric parameters of CNT bundle interconnects on both outputs including power dissipation and propagation delay. The Taguchi results reveal that the length of interconnects has the greatest effect on the performance of SWCNT bundle interconnects (its efficiency is 51% and 47% on the power dissipation and propagation delay, respectively). However, the least effective geometric parameter differs in power dissipation and propagation delay. According to Figure 8 (A), width of interconnects has low impact on the power dissipation (about 7%). And so on, based on Figure 8 (B), diameter of CNTs is the most ineffective parameter (about 11%) on the propagation delay. In summary, the distance between CNTs is in the second rank of importance from performance viewpoint. Next, the Taguchi prediction algorithm was utilized to estimate the performance of desired cases (Table 4). These data were used to perform response surface analysis.

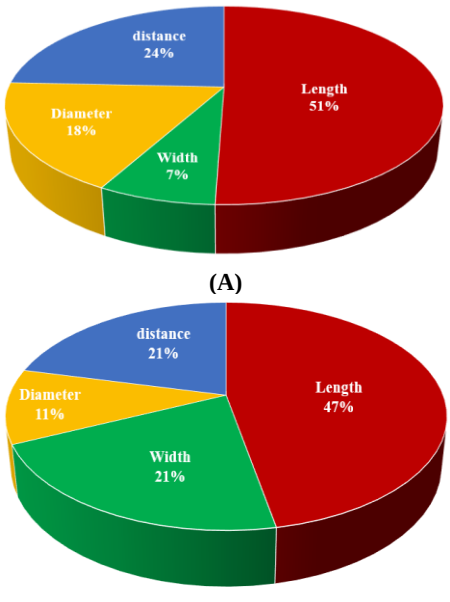

Figure 8. The quantitative effects of geometric parameters of CNT bundle interconnects on the circuit performance including (A) power dissipation and (B) propagation delay

TABLE 4. The estimated circuit performance for different settings of geometric parameters using Taguchi prediction algorithm

Case No.	Length of interconnects, um	Width of interconnects, nm	Diameter of CNTs, nm	Distance between CNTs, nm	Power dissipation, uw	Propagation delay, Ns
1	100	40	2	0.34	1.885	1.779
2	100	50	4	1	1.878	1.762
3	100	30	1	1	1.619	1.769
4	100	30	4	0	2.083	1.765
5	100	50	1	0	1.949	1.757
6	100	50	1	1	1.681	1.762
7	100	50	4	0	2.145	1.757
8	100	30	1	0	1.886	1.764
9	100	30	4	1	1.815	1.769
10	50	50	2	0.34	1.662	1.746
11	50	40	2	0	1.704	1.746
12	50	30	2	0.34	1.599	1.753
13	50	40	4	0.34	1.638	1.767
14	50	40	1	0.34	1.441	1.767
15	50	40	2	0.34	1.581	1.760
16	50	40	2	1	1.436	1.750
17	10	50	1	1	1.123	1.730
18	10	50	4	0	1.587	1.726
19	10	30	1	0	1.328	1.733
20	10	30	4	1	1.257	1.738
21	10	30	4	0	1.525	1.733
22	10	50	4	1	1.320	1.731
23	10	50	1	0	1.390	1.726
24	10	30	1	1	1.060	1.737
25	10	40	2	0.34	1.327	1.747

The results of RSM analysis for power dissipation and propagation delay are displayed in Figures 9 and 10, respectively. It should be noted that in these analyses, the constant parameter was assumed to be the average level value (L2). Eventually, the most significant findings from the RSM contours are:

1. The output of power dissipation also enhances by increasing length of interconnects (L).
2. By increasing both width of interconnects (W) and diameter of CNTs (D), the power dissipation increases. But this development is limited to power dissipation < 1.4.
3. As the distance between CNTs in a bundle (d) decreases, the power dissipation increases.
4.To achieve the highest value of power dissipation, the maximum values for the parameters of length and width of interconnects (L, W), and diameter of CNTs (D) must be considered. Moreover, the distance between CNTs in a bundle (d) should be set to minimum value.
5. It is clear that increasing the length of interconnects (L) will increase the propagation delay.
6. The variations of CNTs' diameter (D) do not have a significant effect on propagation delay. In other words, this parameter is ineffective.
7. There is a specific middle area for both the width of interconnects (W) and the distance between CNTs in a bundle (d) which is relevant to the maximum value of propagation delay. And the propagation delay is reduced by moving away from that area. In other words, the farthest from that area results in the least amount of propagation delay. Moreover, the form of the function is circular between two independent parameters W and d.
8. The lowest propagation delay in the system is achieved when we have the shortest L, d, and maximum W.

Next, the optimization was performed to design a high-performance CNT bundle interconnects in a full adder. This process was performed using a multi-objective function. The optimal values for minimizing power dissipation and propagation delay were obtained simultaneously. Afterwards, the optimal system efficiency was compared using various techniques in Table 5.

Results show that the difference between performance of optimal design of SWCNT bundle interconnects in a full adder predicted by different techniques is less than 6% which is acceptable according to engineering standards.

TABLE 5. Comparison of the optimal system efficiency using various techniques

Parameter	Optimal value	Power delay product (PDP=power dissipation × propagation delay)	
		Taguchi approach	Response surface analysis
L	10 um	Power dissipation = 1.1234	Power dissipation = 1.06097
W	50 nm		
D	1 nm	Propagation delay = 1.73067	Propagation delay = 1.72610
d	1 nm		
Final result		PDP = 1.944	PDP = 1.831

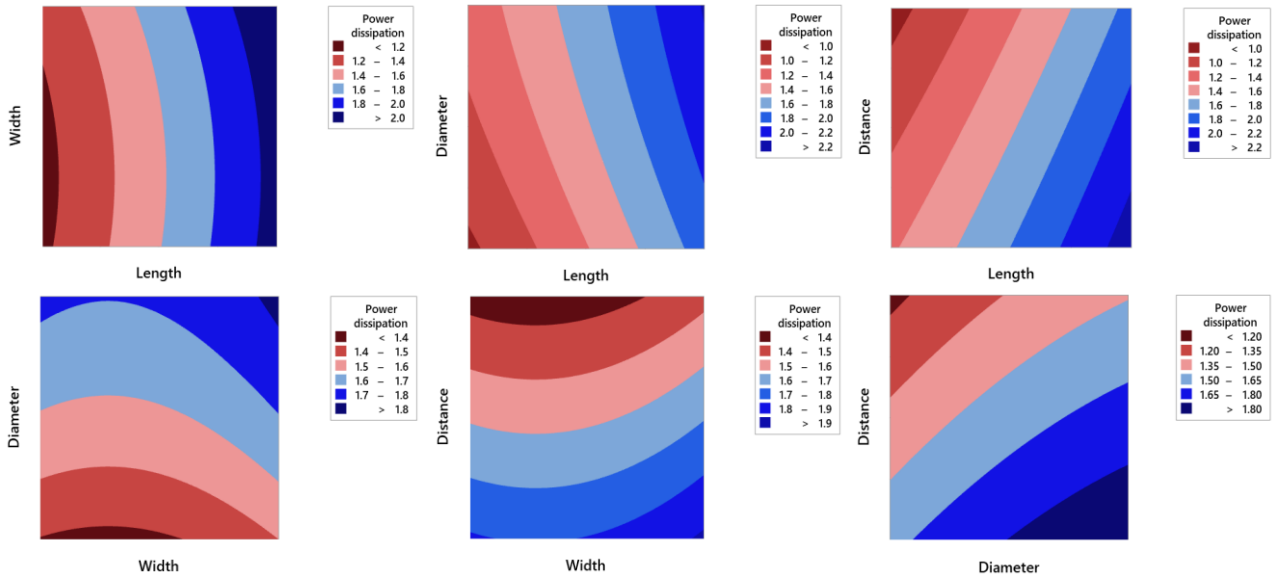

Figure 9. RSM results for power dissipation of the SWCNT bundle interconnects in a full adder

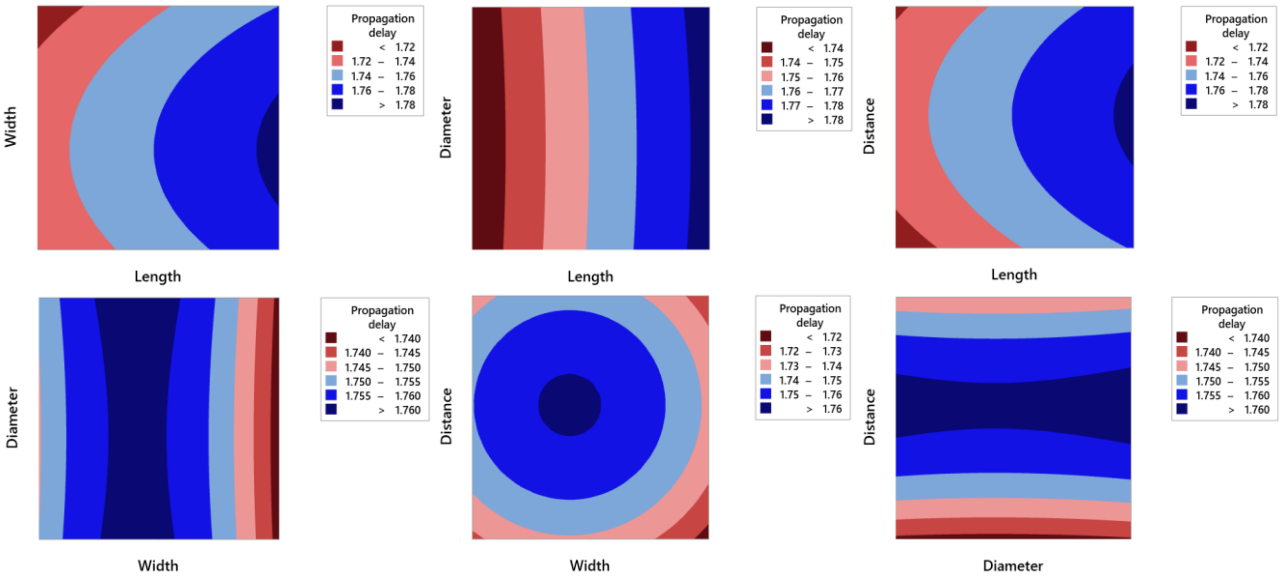

Figure 10. RSM results for propagation delay of the SWCNT bundle interconnects in a full adder

6. CONCLUSION

The current study has attempted to investigate the effects of different geometric parameters of SWCNT bundle interconnects in a full adder on the power dissipation and propagation delay. To achieve this purpose, HSPICE simulation, TA, and RSM were used. Based on the obtained results from all techniques, the parameters of length of interconnects (L), width of interconnects (W), diameter of CNTs (D), and distance between CNTs in bundle (d) were considered as input variables. Also, the power dissipation and propagation delay were considered as performance of the system. Taguchi results indicated that the length of interconnects had the most impact on power delay product (PDP). Next, RSM was used to investigate the interaction impacts of different factors on the circuit performance of carbon nanotube bundle interconnectors in a full adder. In addition, it stated that in order to have the lowest propagation delay in the system, the parameters L and d must be set to the minimum levels and inverse for the parameter W (maximum level of W). Also, the changes in D are ineffective on propagation delay. Eventually, a new design was presented to improve the circuit performance of SWCNT bundle interconnects in a full adder using different data mining techniques such as Taguchi approach and response surface analysis.

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Persian Abstract

چکیده

در پژوهش حاضر، نویسندگان سعی کردند تا به طراحی یک اتصال نانو لوله کربنی تک جداره با کارآیی بالا در یک مدار تمام جمع‌کننده بپردازند. برای دستیابی به این هدف، عملکرد مدار با استفاده از شبیه‌سازی در نرم‌افزار اچ اسپایس و با در نظر گرفتن تکنولوژی ۳۲ نانومتری مورد بررسی قرار گرفت. سپس، اثر پارامترهای هندسی مانند قطر نانو لوله، فاصله بین نانو لوله‌ها در یک باندل، طول و عرض باندل بر توان مصرفی و زمان تاخیر انتشار با استفاده از روش طراحی آزمایش تاگوچی مورد بررسی قرار گرفت. نتایج تحلیل حساسیت تاگوچی نشان داد که طول باندل موثرترین پارامتر در عملکرد مدار است (حدود ۵۱٪ اثرگذاری بر توان مصرفی و ٤٧٪ اثرگذاری بر زمان تاخیر انتشار). پس از آن، فاصله بین نانو لوله‌ها در مقایسه با سایر پارامترها تاثیر بیشتری بر روی پاسخ دارد. همچنین روش پاسخ سطح نشان داد که افزایش طول باندل منجر به افزایش اتلاف انرژی می‌شود. همچنین با افزایش عرض باندل و قطر نانو لوله کربنی، اتلاف انرژی افزایش می‌یابد. کاهش فاصله بین نانو لوله‌های کربنی در یک باندل منجر به افزایش اتلاف انرژی می‌گردد. بدین ترتیب، بیشترین مقدار اتلاف انرژی در صورتی حاصل می‌شود که مقادیر پارامترهای طول و عرض اتصال و قطر نانو لوله کربنی بیشینه و فاصله بین دو نانو لوله حداقل باشد. همچنین نشان داده شد که افزایش طول اتصال منجر به افزایش تاخیر در انتشار می‌شود. در نهایت، پارامترهای بهینه گزارش شد و عملکرد مدار بهینه پیشنهادی با استفاده از روش‌های مختلف (تاگوچی و پاسخ سطح) مقایسه شد. نتایج نشان داد که میزان عملکرد طراحی بهینه اتصال نانو لوله کربنی تک جداره در یک مدار تمام جمع کننده توسط دو روش کمتر از ٦ درصد اختلاف پیش‌بینی شده که مطابق با استانداردهای مهندسی قابل قبول است.